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Small Area Implementation for Optically Reconfigurable Gate Array VLSI: FFT Case

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Optically reconfigurable gate array (ORGA) is a type of multi-context field programmable gate array (FPGA) that has achieved a nanosecond-order reconfiguration capability as well as attaining numerous reconfiguration contexts. Its high-speed dynamic reconfiguration capability is suitable for dynamically changing the function of multi-core processor. ORGA system has high dependability in a radiation rich environment and the development is progressing towards better radiation tolerance. In this paper, size minimization of the ORGA-VLSI is the main concern to maintain its high dependability; hence wire complexity needs special consideration during floor planning. A case of Fast Fourier Transform (FFT) is shown to demonstrate the effectiveness of circuit modification by implementing dynamic reconfiguration for area optimization. Results show that, compared with a normal FFT configuration, the minimum wirelength is reduced 5.5% for a 32-point FFT implementation.

Keywords: Optically Reconfigurable Gate Array, Field Programmable Gate Array, Fast Fourier Transform

Introduction

Dependable system is a recent trend and currently under development by many researchers[1,2]. An application of dependable system is anti-radioactivity in high radiation environment such as in satellites, space stations and nuclear plant. Embedded devices in such situations are vulnerable to the effects of high-energy particles, which leads to Single Event Effect (SEE) where unexpected transition and damage of circuit information may occurs[3,4]. Currently, FPGA for space uses an error checking and correction method (ECC) that can repair the SEE. Nevertheless, in radiation-rich environment, ECCs is not perfect in improving SEEs. Therefore, a circuit on FPGA is always more vulnerable to space radiation than a circuit of an ordinary application-specific integrated circuit (ASIC). This is where optically reconfigurable gate array (ORGA)[5] is expected to play some role due to its fast reconfigurability, that recovers ORGA system not only from SEE, but also from fatal device faults. ORGA, consisting of laser diodes array, holographic memory and gate array VLSI, performs parallel programming capability and support high-speed dynamic reconfiguration with numerous reconfiguration contexts. Studies on radiation tolerance on ORGA system has been performed previously on laser diodes[6] and holographic memory. However, none of these studies focusing on radiation tolerance of the VLSI part. Although, from the viewpoint of radiation tolerance, die size of VLSI should be minimum to reduce chance of receiving neutrons, ORGA has a problem: photo diode to enable fast reconfiguration cannot be made small due to sensitivity issue. Therefore, there will be no further size reduction of gate array architecture and this will limit the resources in terms of number of logic blocks and complex wire segments. Reducing the size of an ORGA-VLSI as much as possible is a critical issue, leading to special considerations on placing registers and routing logic block interconnections. Any adjustment of macroscopic system structure will have a chance to achieve further area decrement. Normal place and route[7] design aid will minimize the area but the area minimization is not fully optimized. Hence, circuit modification is important before usual place and route. In this paper, case of Fast Fourier Transform (FFT)[8] is shown as an example to demonstrate the effectiveness of circuit modification by swapping nodes (swapping registers placement) which reduces the wirelength for an FFT configuration.

Robust ORGA architecture

Gate array structure

A basic ORGA architecture as shown in Figure 1(a) consists of laser diodes array that reads out

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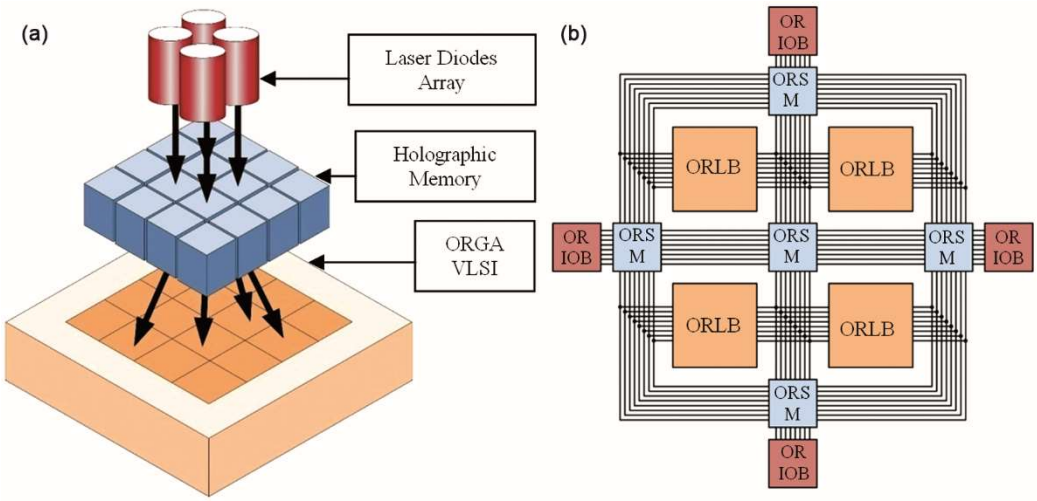

Fig. 1 — (a) Basic architecture of ORGA and (b) block diagram of gate array with 2 x 2 logic blocks

configuration context, holographic memory that stores circuit information and gate array VLSI.

In an ORGA VLSI, photodiodes array is implemented together with programmable gate array and receives the diffraction pattern as a configuration context from the holographic memory. In each ORGA VLSI gate array, the configuration context is stored in toggle-flip-flops and specified to each programming element. The gate array operates based on the configuration context until a next configuration context is optically programmed. For example, when one of the lasers in the laser array is turned on, the laser beam will irradiate a holographic memory at a certain incident angle and the holographic memory will generate a two-dimensional diffraction pattern. The diffraction pattern is served as configuration context and captured by photodiodes array of ORGA VLSI. If another reconfiguration context needed, then another laser will be selected and turned on. The incident angle of the laser beam propagation toward the holographic memory differs from the first laser. Therefore, as in the case of the first laser, the holographic memory generates a different configuration context, which is programmed onto the gate array of ORGA VLSI. These are the optical reconfiguration procedures. Due to the structure of hologram, it enables multiple reconfiguration contexts. Figure 1(b) shows a part of a whole block diagram of a gate array structure having 2 x 2 logic blocks. The gate array structure of an ORGA-VLSI is basically identical to that of standard FPGAs, which is an island-style FPGA[9]. The structure design of the ORGA-VLSI consists of optical reconfigurable logic blocks (ORLB), optical reconfigurable I/O blocks (ORIOB), and optical reconfigurable switching matrices (ORSM). Each configuration bit of these blocks is connected to the reconfiguration circuit with a photodiode. The ORLB consists of a look-up table (LUT), delay flip-flop with a reset function and multiplexers, which optically reconfigure simultaneously using photodiodes. The four-directional ORSM contain transmission gates that are connected with a photodiode through the differential reconfiguration circuit. In this architecture, logic blocks and switching matrices can be programmed simultaneously where the information is supplied from a holographic memory. The I/O block is also reconfigured optically. Each I/O block includes four I/O bits that is controlled using nine photodiodes.

Table 1 — Specifications of the ORGA-VLSI[10].

Technology	0.18 μm double-poly 5-metal CMOS process
Chip size	5.0 x 2.5 [mm]
Photodiode size	4.40 x 4.45 [μm]
Number of photodiodes	10,322
Gate count	2,720

CMOS technology implementation

The ORGA VLSI chips that have been designed and fabricated are using 0.18μm[10] and 0.35μm standard complementary metal oxide semiconductor (CMOS) process technology. Most of the transmission gates and photodiode cells are designed as custom cells referring to size of standard cells. The supply voltages are 1.8V for the core and 3.3V for I/O. This work is done based on the specification of ORGA-VLSI as in Table 1.

System arrangement: FFT case

FFTs are algorithms for a faster calculation of Discrete Fourier Transform (DFT) of a data vector and

reduce the number of computations needed for N points from $O(N^2)$ to $O(N\log_2 N)$. Figure 2(a) shows a signal flow graph of a 2^N-point FFT that consists of radix-2 algorithm as shown in butterfly signal flow of Figure 2(b). The actual implementation is presented as in Figure 2(c), which consists of register and radix-2 butterfly. This FFT implementation demonstrates a good example of dynamic reconfiguration as a method to minimize area of ORGA-VLSI. For example, as in Figure 2(a) three stages of 8-point FFT can be implemented within one stage area of computations. At first, logic blocks are configured according to the first stage of FFT radix-2^N algorithm where N is the number of stages. The logic blocks in the second stage are then configured dynamically within the same area followed by the third stage dynamic reconfigurations. However, later stages of configuration will have longer connections between registers. Hence, long delay in operation is expected to occur as well as larger area will be consumed after place and route because of limited wiring resources. In order to estimate area reduction and improve delay, the wirelength itself is calculated first. The routing path connection is taken into consideration according to complex addition and multiplication of an FFT. The wirelength, $w_{(i)(j)}$ is calculated at each input node as in Eq. (1). As in Figure 2(b), the vertical distance between input node and output node is represented by the unit distance, *a,* and horizontal distance between two output node is represent by the unit distance, *b*. The node position is represent as $pos_{(j)}(i) = (x_{(j)}(i), y_{(j)}(i))$ *where* $i = 0,1,\ldots,2^N-1$ for vertical position and $j = 0,1,\ldots N-1$ for horizontal position. For example, by referring to Figure 2(b), if $pos_{(j)}(i) = 0$, $pos_{(j)}(i) = 0$ and $pos_{(j)}(i) = -1$, then, the total unit distance will be $w_{(i)(j)} = a + (a^2 + b^2)^{1/2}$. The output position that depends on *y*-coordinate are differentiated by s, where $s = (-1)^i 2^j$. The total path for each stage are computed by adding all the wirelength distance for each node in vertical position as in Eq. (2). The summation of all vertical wirelength gives the total routing wirelength as in Eq. (3).

$$w_{(i)(j)} = \frac{\sqrt{\left[\left(x_{(j+1)}(i) - x_{(j)}(i)\right) \times a\right]^2 + \left[\left(y_{(j+1)}(i) - y_{(j)}(i)\right) \times b\right]^2}}{\sqrt{\left[\left(x_{(j+1)}(i+s) - x_{(j)}(i)\right) \times a\right]^2 + \left[\left(y_{(j+1)}(i+s) - y_{(j)}(i)\right) \times b\right]^2}} \quad \ldots (1)$$

$$w_{(j)} = \sum_{i=0}^{2^N-1} w_{(i)(j)} \quad \ldots (2)$$

$$total\ w = \sum_{j=0}^{N-1} w_{(j)} \quad \ldots (3)$$

The initial idea is to reduce wirelength by swapping nodes of the FFT configuration. For example, referring to Figure 2(a), if two of the nodes (second and third node) in the second stage being swapped (denoted by blue arrow), the third node will be closer to the first node and second node will be closer to fourth node. This will give a shorter wirelength at that stage. Therefore, the total wirelength may give further reduction if two or more nodes being swapped. This means that there may be other possibility of other configuration can achieve minimum wirelength compared to normal configuration. Therefore, all possible nodes (register) placement on each stage of 2^N-point FFT was taken into consideration by applying permutation of nodes on all stages.

Experimental results

After all the permutations of nodes are considered on each stage of 2^N-point FFT, the minimum wirelength is observed and demonstrated as in configuration of Figure 3(a). Swapping of nodes happen between stage 2 and stage 3. The calculation of

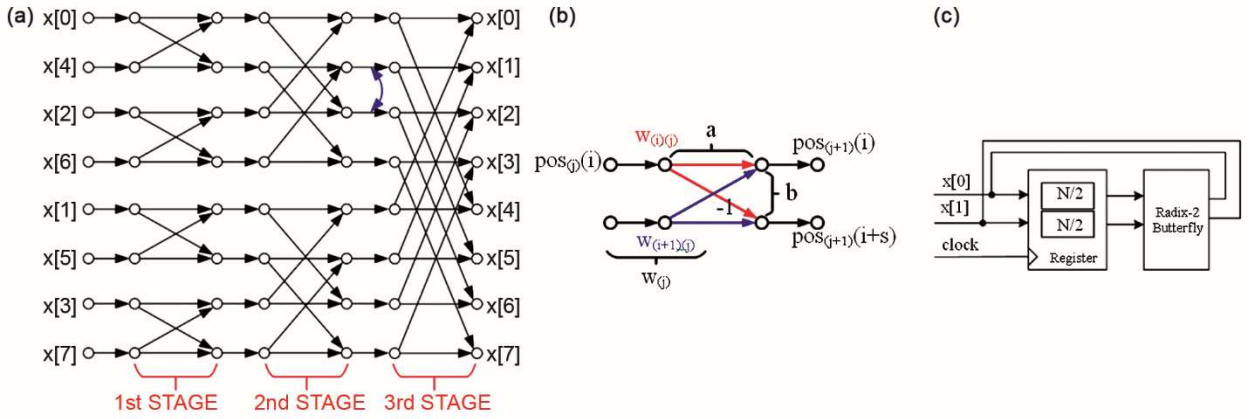

Fig. 2 — (a) An example of a 2^N-point FFT signal flow (b) butterfly signal flow and (c) actual implementation

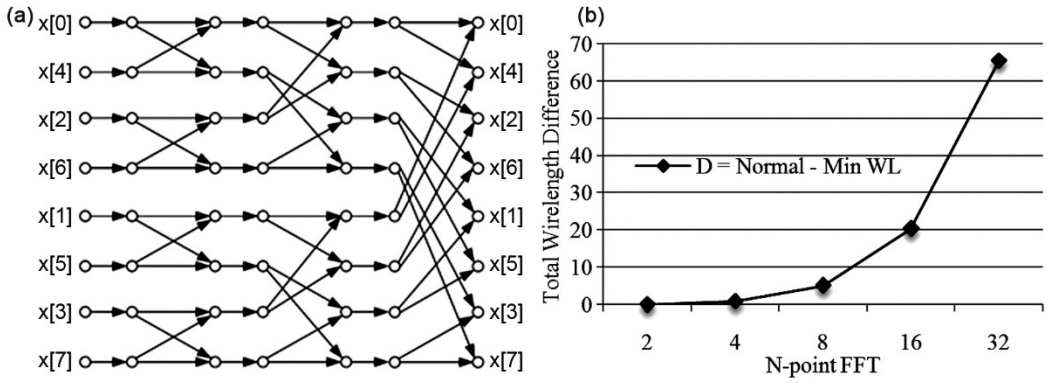

Fig. 3 — (a) Difference of minimum configuration compared to normal configuration for 2^N-point FFT and (b) signal flow graph of minimum WL configuration of 8-point FFT computation

Table 2 — Wirelength calculation of 2^N-point FFT.

2^N-point FFT	Normal	Minimum WL
2	4.8284	4.8284
4	22.6011	21.7858
8	86.1871	81.0681
16	317.3703	297.0153
32	1179.7397	1114.2373

wirelength is performed from 2-point FFT up to 32-point FFT. Table 2 shows the wirelength values for the normal and minimum wirelength (minimum WL) configuration of FFT. The increment number of normal wirelength shows that more number of stages due to higher 2^N-point FFT gives longer wire. The minimum WL is compared with normal configuration and represented as D (D=Normal-Minimum WL) in Figure 3(b) graph. For a 32-point FFT, minimum WL gives a 5.5% wirelength reduction. By extrapolating the results, the percentage reduction is expected to increase when data points are more than 64, which is under investigation due to long computation time in generating permutations.

Conclusion

This paper concerns for fast reconfiguration time and high dependability of an ORGA system. Many points such as high-speed dynamic reconfiguration and macroscopic floor planning in a programmable gate array are very important to achieve nanosecond-order reconfiguration capability even in a high radiation environment. The proposed approach has achieved 5.5% wirelength reduction in comparison to normal FFT configuration and lowers the possibility of wire complexity. It is expected that the higher 2^N-point FFT, larger wirelength difference will be achieved. The future work of this research is to focus on more advanced dependability-increasing technique. Therefore, there will be indistinct boundary performance between ORGA, FPGA and 3-D integrated circuit.

References

1 Yazdanshenas S, Asadi H & Khaleghi B, A Scalable Dependability Scheme for Routing Fabric of SRAM-Based Reconfigurable Devices, *J IEEE Trans VLSI Syst,* **23** (2014) 1868-1878.

2 Alho P & Mattila J, Breaking Down the Requirements: Reliability in Remote Handling Software, *J Fusion Eng Des,* **88** (2013) 1912-1915.

3 Benfica J, Green B, Porcher B C, Poehls L B, Vargas F, Medina N H, Added N, Aguiar V A P, Macchione E, Aguiire F, Selveira M, Perez M, Haro M S, Sidelnik I, Blosteon J, Lipvetzky J & Bezerra E A, Analysis of SRAM-Based FPGA SEU Sensitivity to Combined EMI and TID Imprinted Effects, *J IEEE Trans Nucl Sci* **63** (2016) 1294-1300.

4 Virmontois C, Toulemont A, Rolland G, Materne A, Lalucaa V, Goiffon V, Codreanu C, Durnez C & Bardoux A, Radiation-Induced Dose and Single Event Effects in Digital CMOS Image Sensors, *J IEEE Trans Nucl Sci,* **61** (2014) 3331-3340.

5 Tanigawa A & Watanabe M, Dependability-increasing Technique for a Multi-context Optically Reconfigurable Gate Array, *Proc IEEE Int Symp Circuits Syst,* (2013) 1568-1571.

6 Fujimori T & Watanabe M, Radiation Tolerance of Color Configuration on an Optically Reconfigurable Gate Array, *Proc IEEE Int Parallel Distrib Process Symp Work,* (2014), 205–210.

7 Vansteenkiste E, Al Farisi B, Bruneel K & Stroobandt D, TPaR: Place and Route Tools for the Dynamic Reconfiguration of the FPGA's Interconnect Network, *J IEEE Trans Comput-Aided Design Integr Circuits Syst,* **33** (2014) 370-383.

8 Vennila C, Lakshminarayanan G & Ko S, Dynamic Partial Reconfigurable FFT for OFDM Based Communication Systems, *J Circuits Syst Signal Process,* **31** (2012) 1049–1066.

9 Baig H & Lee J, An Island-style-routing Compatible Fault-Tolerant FPGA Architecture with Self-Repairing Capabilities, *Proc Int Conf Field-Programmable Tech,* (2012) 301-304.

10 Kubota T & Watanabe M, 0.18μm CMOS Process Photodiode Memory, *Proc IEEE Int Symp Circuits Syst,* (2013), 1464–1467.