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Low-voltage variable current gain CCII based all-pass/notch filter

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A second order low-voltage current conveyor type II (CCII) based filter circuit which can realize dual filter functions (all-pass/notch) depending on the current gain of CCII has been presented. The circuit employs equal valued components with all capacitors grounded and is more suitable for chip implementation. The circuit offers high input impedance, low output impedance and employs same type of active devices (CCII+). Theoretical results have been validated by PSpice simulations using 0.5 μm technology parameters at supply voltage of ± 0.75 V.

Keywords: Low-voltage circuits, Current conveyor, Active filter

1 Introduction

A CCII is the most versatile circuit building block that has been widely used in filters and inductance realizations due to its performance superiority over the conventional op amps[1-10]. Filters being important constituents of modern communication and instrumentation systems need to be operated with low supply voltages. The low-voltage CCII can be designed by employing low-voltage circuit design techniques[11-13]. The use of floating gate MOSFET (FGMOS) is one such technique where the effective threshold voltage can be lowered than its conventional value and the resulting circuits can be operated at low supply voltage[14-18].

A number of all-pass/notch filter circuits have been reported earlier having the advantage of high input impedance or grounded capacitors[19-29]. In order to realize a high input impedance filter which makes circuit suitable for cascading to obtain higher order filters and also having the advantage of grounded capacitors, the task becomes difficult if one is restricted to two current conveyors. In this paper, all-pass/notch filter realized using a low-voltage FGMOS based CCII is presented. The circuit described here is different from the several voltage mode all-pass/notch filter circuits reported earlier as it uses a variable current gain CCII with grounded capacitors and offers high input impedance. As compared to the recent circuit[30], which describes a first order all-pass filter using almost the same number of active and passive components (capacitors), the proposed circuit realizes second order dual filter functions. The operation of these circuits has been verified by using PSpice simulations for 0.5 μm technology at ± 0.75 V.

2 Circuit Description

The circuit for the all-pass/notch filter using CCII with variable current gain is shown in Fig. 1. The circuit yields the following biquadratic transfer function (T F) for CCII+ having $I_Y = 0$, $V_X = V_Y$ & $I_Z = K I_X$.

$$\frac{V_o(s)}{V_{in}(s)} = n\left[\frac{s^2 C_2 C_3 R_2 R_3 + s(C_2 R_2 + C_3 R_3 - K C_2 R_3) + 1}{s^2 C_2 C_3 R_2 R_3 + s(C_2 R_2 + C_3 R_3) + 1}\right] \quad \ldots (1)$$

where K is the current gain of CCII+ and n is the resistance-scaling factor.

Eq. (1) gives center frequency, $\omega_0 = \frac{1}{\sqrt{C_2 C_3 R_2 R_3}}$ and quality factor as: $Q = \frac{\sqrt{C_2 C_3 R_2 R_3}}{C_2 R_2 + C_3 R_3}$

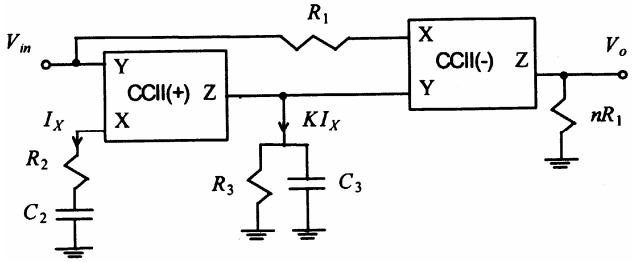

Fig. 1— All-pass/notch filter

The filter circuit has low values of sensitivity to component variations as revealed by the following sensitivity analysis:

$$S_{C_2}^{\omega_0} = S_{C_3}^{\omega_0} = S_{R_2}^{\omega_0} = S_{R_3}^{\omega_0} = -\frac{1}{2} \quad \ldots (2)$$

$$S_{C_2}^{\frac{\omega_0}{Q}} = S_{R_2}^{\frac{\omega_0}{Q}} = -\frac{C_3R_3}{C_2R_2 + C_3R_3} \quad \ldots (3)$$

and $S_{C_3}^{\frac{\omega_0}{Q}} = S_{R_3}^{\frac{\omega_0}{Q}} = -\frac{C_2R_2}{C_2R_2 + C_3R_3}$ … (4)

Now if we select $K = \frac{R_2}{R_3} + \frac{C_3}{C_2}$, Eq. (1) gives a T F for notch response as :

$$\frac{V_o(s)}{V_{in}(s)} = n\left[\frac{s^2C_2C_3R_2R_3 + 1}{s^2C_2C_3R_2R_3 + s(C_2R_2 + C_3R_3) + 1}\right] \quad \ldots (5)$$

By selecting equal valued components for simplicity, that is for $R_2 = R_3 = R \;\&\; C_2 = C_3 = C$, Eq. (5) becomes

$$\frac{V_o(s)}{V_{in}(s)} = n\left[\frac{s^2C^2R^2 + 1}{s^2C^2R^2 + 2sCR + 1}\right] \quad \ldots (6)$$

which gives center frequency $f_0 = \frac{1}{2\pi RC}$ *and* $Q = 0.5$.

Similarly for $K = 2\left(\frac{R_2}{R_3} + \frac{C_3}{C_2}\right)$, Eq. (1) yields T F for all-pass response as:

$$\frac{V_o(s)}{V_{in}(s)} = n\left[\frac{s^2C_2C_3R_2R_3 - s(C_2R_2 + C_3R_3) + 1}{s^2C_2C_3R_2R_3 + s(C_2R_2 + C_3R_3) + 1}\right] \quad \ldots (7)$$

and for equal valued components, T F is as shown below:

$$\frac{V_o(s)}{V_{in}(s)} = n\left[\frac{s^2C^2R^2 - 2sCR + 1}{s^2C^2R^2 + 2sCR + 1}\right] \quad \ldots (8)$$

The phase shift (φ) is given as:

$$\varphi(\omega) = -2\tan^{-1}\left(\frac{2\omega CR}{1-(\omega CR)^2}\right) \quad \ldots (9)$$

The current gain (K) of CCII+ controls the filter function and resistance-scaling factor (n) controls the filter gain. However, the circuit shown in Fig. 1 has a disadvantage of having low input impedance due to resistance R_1 besides employing two CCIIs of different polarities. The output impedance is also not low as it depends upon resistance nR_1. These drawbacks can be overcome by modifying the circuit of Fig. 1 by using voltage buffers and retaining the same performance, as shown in Fig. 2. Now, the circuit of Fig. 2 has high input impedance, low output impedance and employs the same type of CCIIs.

3 Simulation Results

3.1 CCII

CCII+ used for realizing circuit in Fig. 2 is taken from Ref. (13) wherein FGMOS current mirrors[15-16] have been used in place of low-voltage current mirrors as shown in Fig. 3. The resultant circuit has been simulated using PSpice for 0.5 μm technology at ± 0.75 V. The threshold voltages for NMOS and PMOS transistors are 0.62 and -0.58 V respectively. The *W/L* ratios for various transistors have been chosen as 25 μm/0.5 μm for M1 and M2, 4 μm/0.5 μm for M4, M6 and M7, 45 μm/1 μm for M8 and M10, 66 μm/1 μm for M3 and M9, and 12 μm/0.5 μm for M5. Simulation results show that the proposed CCII offers an input resistance of 2.53 Ω at port *X*, 10^{20} Ω at port *Y* and output resistance of 119.8 MΩ at port *Z*. The power consumed by the circuit is 1.62 mW. Current and voltage transfer ratios are almost unity with an error less than ± 0.2 %. The bandwidth for both current and voltage transfer has been found to be 100 MHz.

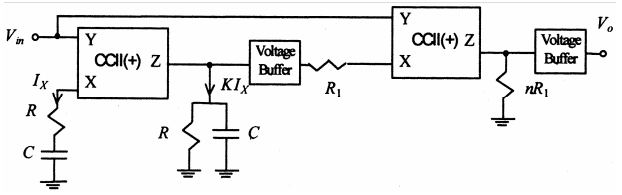

Fig. 2 — Modified all-pass/notch filter

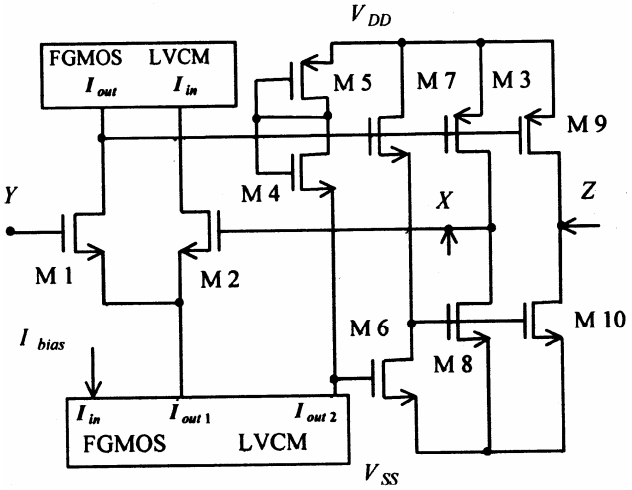

Fig. 3 — CCII+ circuit

It may be mentioned here that by controlling *W/L* ratio of transistors in current output stage in Fig. 3, a variable current gain CCII+ can be obtained. The current gain is obtained by increasing the aspect ratio of transistors M9 and M10 with respect to M3 and M8 in Fig. 3. The current transfer characteristics of variable gain CCII+ are shown in Fig. 4.

3.2 FGMOS voltage buffer

FGMOS current mirrors[15-16] have been used to realize a voltage buffer[14] as shown in Fig. 5. It is simulated by choosing *W/L* ratio of M1 and M2 as 25 µm/1 µm and 120 µm/1 µm for M3 with I_{bias} equal to 50 µA. The dc voltage transfer takes place from 0.75 to 0.69 V with error within ± 2.5 % (Fig. 6). The bandwidth of the circuit is about 60 MHz as shown in Fig. 7. The input resistance offered is 3×10^{11} Ω, output resistance is 1.46 Ω and the power consumed is 1.14 mW.

Now the circuit of Fig. 2 is simulated to yield notch response (K = 2) with center frequency 3.18 MHz by choosing R = 5 kΩ, R_1 = 5 kΩ and C = 10 pF. The circuit offers an input resistance of 10^{20} Ω, output resistance is 1.4 Ω and the power consumed is 6.82 mW. The simulated magnitude and phase responses of notch filter for different gains are shown in Figs 8(a) and (b) respectively.

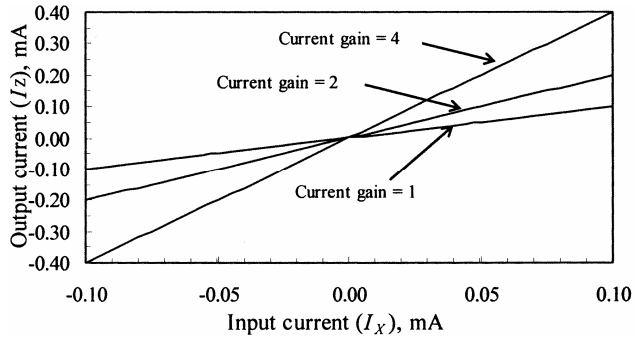

Fig. 4 — Current transfer characteristics of CCII+ with gain

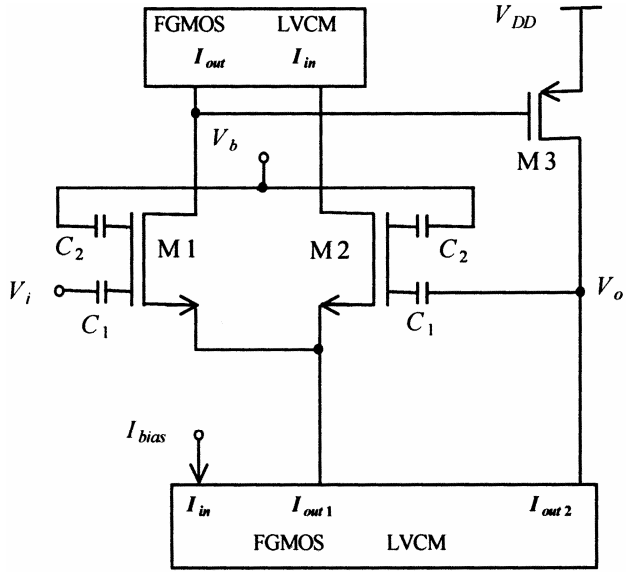

Fig. 5 — FGMOS voltage buffer

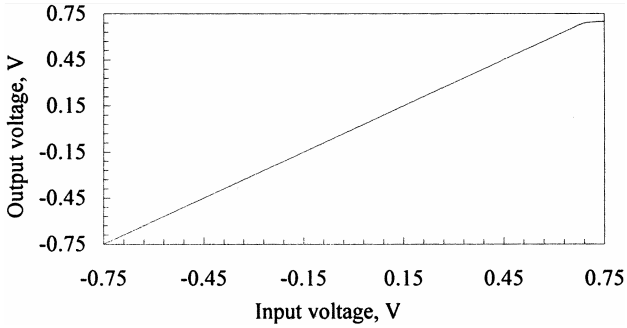

Fig. 6 — DC voltage transfer characteristic of voltage buffer

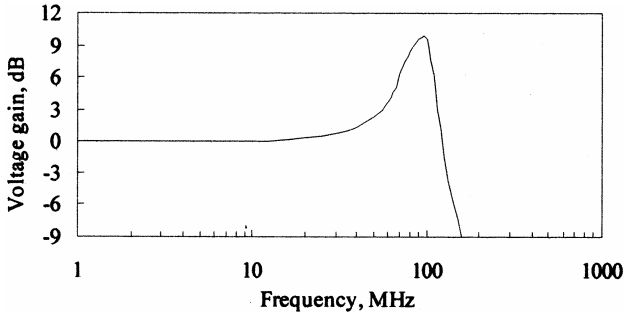

Fig. 7— Frequency response of voltage buffer

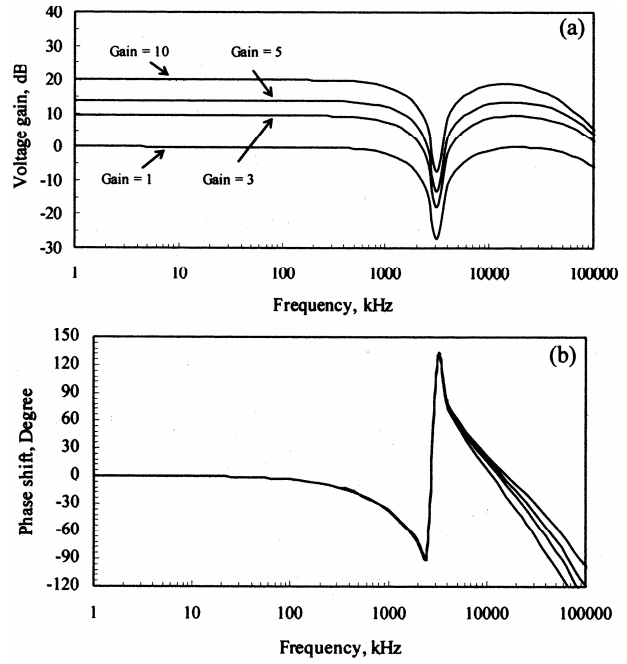

Fig. 8— (a) Magnitude response of notch filter; (b) Phase response of notch filter

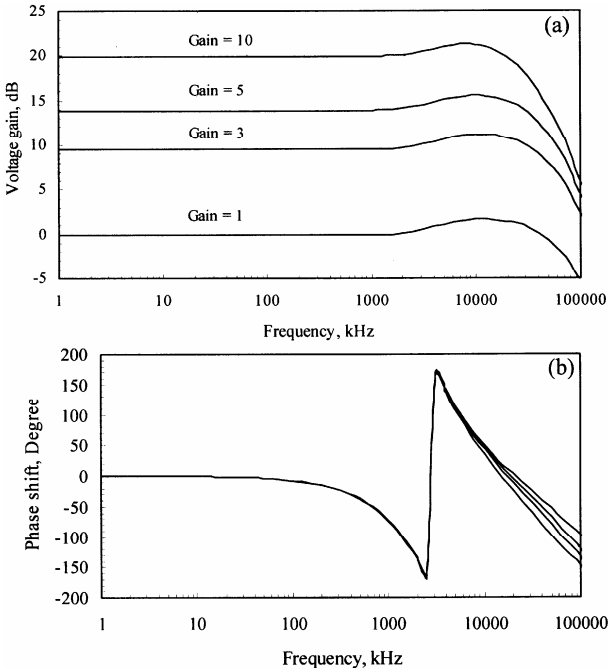

Fig. 9— (a) Magnitude response of all-pass filter; (b) Phase response of all-pass filter

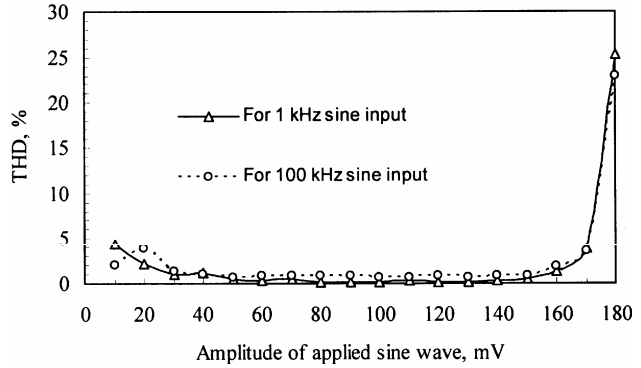

Fig. 10 — THD plot

For $K = 4$, all-pass response is obtained as shown in Figs 9(a) and (b). It has been observed that the simulated response of the filter deviates at higher frequency due to the limitations and non-idealities of CCIIs used. The total harmonic distortion (THD) has also been calculated as a function of amplitude of the input sinusoidal signal for different frequencies as shown in Fig. 10. It has been observed that THD remains well below 5 % upto 170 mV amplitude of input signal.

4 Conclusions

A simple low-voltage variable current gain CCII based filter circuit that can realize both notch and all-pass filter responses has been presented. The circuit offers high input impedance, low output impedance, employs two current conveyors of same type besides grounded capacitors and thus make it suitable for IC implementation. These circuits can operate with a supply voltage of ± 0.75 V and exhibit low value of THD. The simulation results verify the theory.

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