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Structure and performance of a new data clock time recovery phase locked loop

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A new phase locked loop (PLL)-based data clock recovery circuit having non-linear error control characteristics has been proposed. Its performance has been studied by analytical means, by numerically solving the system eqution using computer, and by hardware experiment in the radio frequency band. Different performance-measuring parameters of the system such as acquisition range and transient response time obtained by different methods confirm the improved response of the proposed circuit compared to the conventional system.

Among various applications of the phase locked loops (PLLs) in communication system, the extraction of the timing signal from the received data stream is one[1-3]. In the PLL-based data clock recovery circuits, the use of Hogge PD has been recently suggested[4]. It offers saw-tooth-type error control characteristics which helps to get large acquisition range of the loop. However, if the error transfer characteristic of the PD can be properly modified one can enhance the speed of operation as well as acquisition range of the loop. In this paper, a modified PLL-based clock-recovery circuit, using a Hogge-type PD followed by a non-linear amplifer has been proposed. The non-linearity in the loop amplifier gain characteristics provides large control voltage for higher phase errors and thus enhances the speed of the transient response of the modified system. The proposed circuit performance has been studied analytically using the suitable mathematical model of the loop. Moreover, the system equation has been numerically solved using computer. A prototype hardware circuit of the proposed system has also been tested in the radio frequency band.

Hardware Structure

Fig. 1a shows the block diagram of the proposed circuit which is different from the conventional structure having an additional non-linear amplifier (NLA), inserted between the PD and the loop filter. The Hogge PD used in the loop provides a saw-tooth type error voltage. Figs 1b and 1c show, respectively, the hardware circuits of the PD and the NLA used in the proposed system. The circuit (Fig. 1b) compares the phases of the delayed data and the clock. When a change in the state of the delayed data takes place, the D input and the Q output of the first D type flip-flop are no longer same. So, output of the first XOR gate U1 is high and it remains high until the rising edge of the next clock. At the same time the D input and Q output of the second D-type flip-flop U4 are unequal, so the output of second XOR gate U2 would go high and remains so until the falling edge of the next clock. Finally the phase error can be obtained by comparing the width of the output pulses of U1 and U2. The variation of the average output of this PD with phase error is sawtooth in nature and it has linear range from $-\pi$ to $+\pi$.

From Fig. 1c, the structure of the NLA can be understood. It has been realised using a conventional operational amplifier along with non-linear circuit elements, such as antiparallel p-n junction diodes, shunted by a suitable resistor. It has been observed that the output of constructed NLA can be expressed as a power series of the input. In the limit of moderate input voltage, the linear and the cubic power terms of the input would be sufficient to express the output of the NLA. The low pass filtered version of the NLA output is used as the control signal of the voltage controlled oscillator (VCO).

Mathematical Model

It is known that the Hogge PD shows a saw-tooth type error transfer characteristics. Hence the data clock recovery loop can be modelled as a phase locked loop having a saw-tooth type PD in

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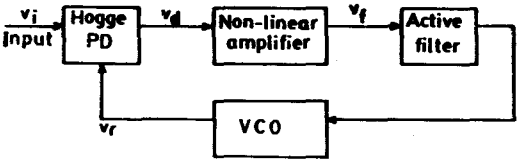

Fig. 1a—Block diagram of the proposed PLL based clock recovery circuit

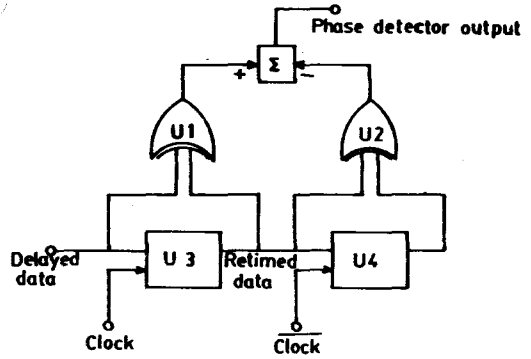

Fig. 1b—Circuit diagram of the Hogge PD

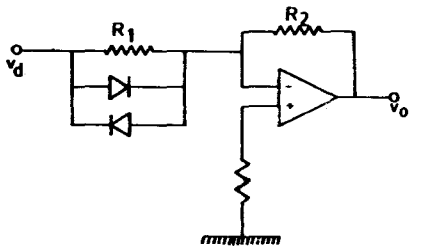

Fig. 1c—Circuit diagram of the non-linear amplifier

it. The effect of inclusion of a NLA in the data clock recovery circuit could be analysed by studying the response of a continuous wave (CW) PLL consisting of a saw-tooth PD followed by the NLA under consideration. To find out acquisition behaviour of a CW PLL having a saw-tooth PD, with and without NLA in the system, consider the received input signal ($v_i(t)$) and the local reference VCO signal ($v_r(t)$) as

$$v_i(t) = A \sin(w_i t + \theta_i) \quad \ldots (1)$$

and

$$v_r(t) = 2\cos(w_r t + \hat{\theta}) \quad \ldots (2)$$

Here ($A^2/2$), $w_i (= 2\pi f_i)$ and θ_i are, respectively, the power, angular frequency and the phase of the input signal; $w_r (= 2\pi f_r)$ and $\hat{\theta}$ are, respectively, the angular frequency and the phase of the VCO.

Considering the saw-tooth characteristics of the PD, its output $v_d(\phi)$ (which is proportional to the phase error between $v_i(t)$ and $v_r(r)$) can be written as

$$v_d(\phi) = K_p \sum_{n=1}^{\infty} C_n \sin n\phi \quad \ldots (3)$$

where

$$\phi = (w_i - w_r)t + \theta_i - \hat{\theta} \quad \ldots (3a)$$

and

$$C_n = (-1)^{n+1} \frac{2}{n\pi} \quad \ldots (3b)$$

K_p depends upon the amplitude of both the input signal of the PD and on the PD response and is expressed in volts per radian. The experimental input-output characteristics of the NLA used has been shown in the inset of Fig. 2 which shows that when the input to the NLA (v_d) is not very high, the output of the NLA (v_f) can be expressed as

$$v_f = K_d v_d + K_a v_d^3 \quad \ldots (4)$$

where K_d and K_a are the amplifier design parameters. The computed variations v_f with v_d for different values of the design parameters has also been shown in the inset of the Fig. 2. For the system under consideration the power series representation upto cubic term of the NLA is reasonable if the output of the loop phase detector be restricted within nearly 0.7 volt. The effect of the NLA with this cubic non-linearity in the system response has been studied. Using Eq. (3) and after simplification, the baseband (low frequency) output of the NLA can be obtained as,

$$v_f = K_p K_d [A_1 \sin\phi + A_2 \sin 2\phi] \quad \ldots (5)$$

where,

$$A_1 = C_1 + \tfrac{3}{4} K_n K_p^2 \{C_1^3 + 2C_1(C_2^2 + C_3^2) + C_3(C_2^2 - C_1^2)\} \quad \ldots (5a)$$

where,

$$A_2 = C_2 + \tfrac{3}{4} K_n K_p^2 \{C_2^3 + 2C_2(C_1^2 + C_3^2) + 2C_1 C_2 C_3\} \quad \ldots (5b)$$

and

$$K_n = K_a / K_d . \quad \ldots (5c)$$

Consider a proportional plus integrating loop filter with transfer function written as

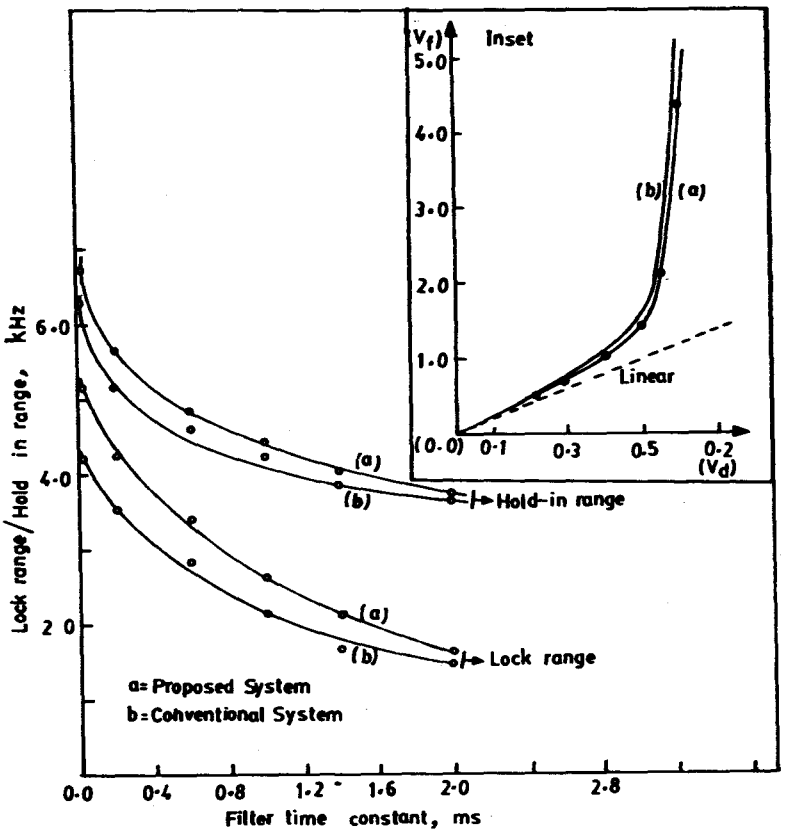

Fig. 2—Experimental variation of the acquisition range and the Hold-in range of the proposed and the conventional system with the filter time constants. [Centre frequency of the VCO = 67.5 kHz, Input voltage = 3.8 volt]. Inset:Input-output characteristics of the NLA considered. (a) Experimental, (b) Computed

$$F(s)=\frac{1+SF_0T}{1+ST}=F(w)\exp(-j\psi(w)) \qquad \ldots(6)$$

where

$$F(w)=[\{1+(wF_0T)^2\}/\{1+(wT)^2\}]^{1/2} \qquad \ldots(7a)$$

and

$$\psi(w)=\arctan[wT(1-F_0)/(1+w^2T^2F_0)] \qquad \ldots(7b)$$

$s(=jw)$ is the complex frequency, F_0 and T are, respectively, the asymptotic high frequency gain and time constant of the filter. Combining Eqs (3a), (5) and (6) and after simplification[5], the phase governing equation of the PLL incorporating saw-tooth PD followed by the NLA becomes,

$$\frac{d^2\phi}{dT^2}=\frac{1}{T_f}[\Omega_n-A_1\sin\phi-A_2\sin2\phi]-[1+F_0T_fA_1\cos\phi+2F_0T_fA_2\cos2\phi]\frac{d\phi}{dT} \qquad \ldots(8)$$

where $T_f(=KT_0)$ and $T(=Kt)$ are, respectively, the normalised filter time constant and the normalised time. $K(=K_pK_dK_0)$ and K_0 are the loop gain and the VCO sensitivity, respectively; $\Omega_n(=(w_i-w_r)/K)$ is the normalised open loop frequency error.

Analytical and Numerical Studies

The response of the system can be examined with the help of Eq. (8). It is extremely difficult, if not impossible, to get a closed form analytical solution of this non-linear equation. So it has been tried to get its numerical solution using a computer and some important conclusions are obtained regarding its acquisition behaviour and transient response speed. The effect of the NLA in the circuit is studied by assigning different values of the non-linear parameter K_n. When $K_n=0$, the system reduces to the conventional PLL with saw-tooth PD. The results of numerical solution have been presented in Fig. 3 which gives the time development of the loop phase error in the face of frequency step input signal. It shows that the circuit incorporating the NLA is able to follow the input

Table 1—Variation of acquisition range with loop filter parameters and NLA parameters

	$F_0=0$			$F_0=0.2$		
T_f	$K_n=0$	$K_n=0.5$	$K_n=1.23$	$K_n=0$	$K_n=0.5$	$K_n=1.23$
	$(\Omega_n)_{max}$	$(\Omega_n)_{max}$	$(\Omega_n)_{max}$	$(\Omega_n)_{max}$	$(\Omega_n)_{max}$	$(\Omega_n)_{max}$
1	0.832	1.085	1.361	0.835	1.080	1.422
5	0.675	0.821	1.023	0.747	0.945	1.248
10	0.611	0.740	0.922	0.723	0.930	1.254
100	0.469	0.542	0.740	0.800	1.121	1.540

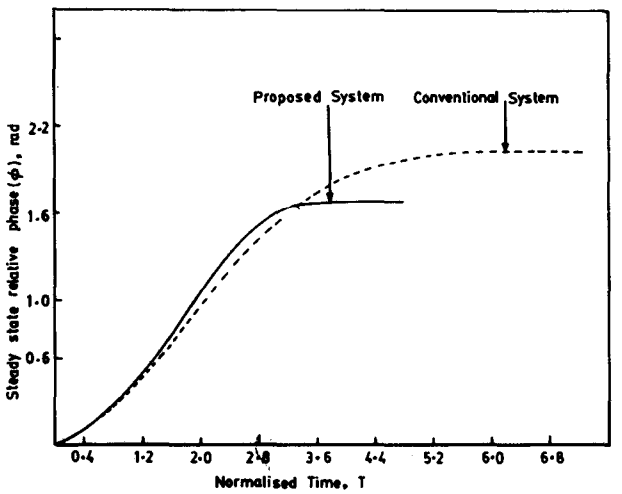

Fig. 3—Time development of the relative phase of the VCO with respect to the input signal for conventional as well as proposed system ($F_0=0$, $\Omega_n=0.8$, $T_f=1$)

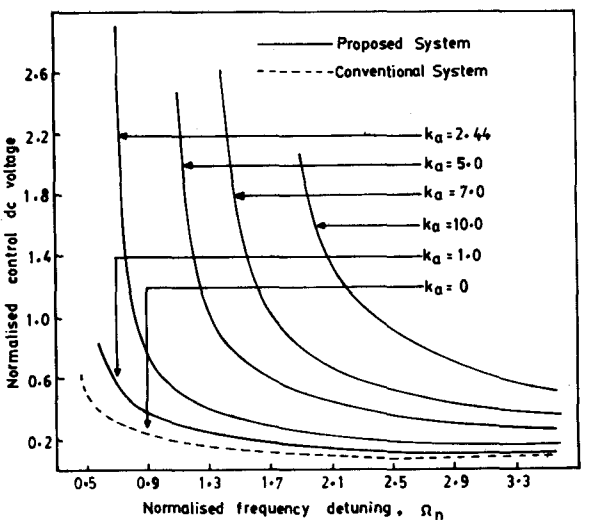

Fig. 4—Variation of the normalised control dc with the open loop normalised frequency detuning for different nonlinearity parameters [$T_f=0.1$, $F_0=0$]

signal phase with greater speed than that of the circuit without NLA. The comparative acquisition behaviour of the systems with and without NLA have been studied numerically by finding steady state solution of Eq. (8). Table 1 represents the maximum frequency detuning (Ω_n) between the signal and the reference upto which the loop can acquire the input signal. Ω_n values have been obtained for different non-linearity parameters, asymptotic high frequency gain factors and filter time constants. From these results it is clear, the proposed system has better acquisition property compared to that of conventional one.

As the dc part of the loop error control voltage (V_{dc}) is responsible for bringing the VCO to the locked state, it is possible to predict the acquisition performance of a phase lock loop by examining the variation of V_{dc} with open loop frequency error (Ω) in the unlocked state. It is known[6] that in the beating condition ($\Omega > K$) of the loop VCO, the output of the PD contains a dc term and a large number of harmonic components of frequency Ω. These components after being amplified by the loop amplifier and passing through the loop filter, shifts the VCO frequency and also frequency modulates it. As F_0 is very small and T_0 is large, it is reasonable to take the output of the VCO in this condition as

$$v_r(t)=2\cos[(w_0+\Delta)t-m\cos(\Omega_1 t+\psi(w))] \quad \ldots (9)$$

Here $\Omega_1(=\Omega-\Delta)$, m and $\psi(w)$ are, respectively, the closed loop frequency error, the VCO phase modulation index and the phase shift due to loop filter. It may be noted that Δ is the dc frequency shift of the VCO in the closed loop condition. Using the mathematical expressings of input signal, VCO reference signal, PD transfer characteristics, NLA response and the loop filter transfer function given in Eqs (1), (9), (3), (4) and (6), respectively, one can find out[6] the variation of the dc component of the VCO control voltage (V_{dc}) with the open loop frequency error (Ω). The computed results are shown in Figs 4 and 5. Fig. 4 shows this variation for different NLA parameters while Fig. 5 shows it for different filter time constants. It is, therefore, clear that by suitably adjusting the NLA parameters, it is possible to improve the acquisi-

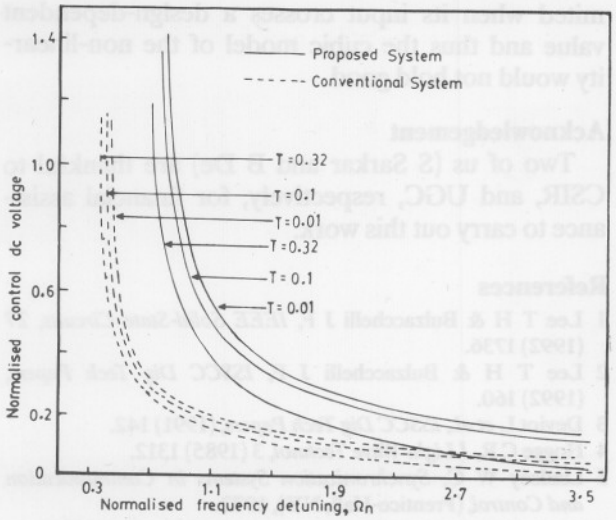

Fig. 5—Variation of the normalised control dc of the proposed and the conventional system with the open loop normalised frequency detuning for different normalised filter time constants [$F_0 = 0$, $K_n = 1.2286$]

tion performance of the proposed system with NLA.

Experimental Studies on the Proposed Loop

The effectiveness of the proposed structure modification algorithm has been verified by a hardware experimental performed in the RF band. The block diagram of the experimental set-up and the actual circuit used for the PD and the NLA are shown in Fig. 1. The loop filter used in this experiment is an imperfect integrator in nature. The 4046 B chip has been used to implement the loop VCO and the centre frequency of the VCO is taken as 67.5 kHz. The input data stream has been simulated using suitable divider circuits and PN sequence generators. Fig. 2 shows the experimental variation of the lock range and the hold-in range of the conventional as well as of the proposed system with different filter time constants. In the inset of the Fig. 2 the transfer characteristic of the NLA used in the circuit has been shown. From the obtained results one may conclude that the proposed system has a better acquisition performance than the conventional one. This helps to recover the clock signal from the received data stream when the detuning of the input data clock frequency from the VCO frequency is greater compared to the same for a conventional system.

To examine the acquisition speed of the proposed system, a data stream whose clock signal frequency is being shifted with the help of a square wave signal (FSK signal) has been used as the loop input signal and the loop error control signal in the clock recovery system has been noted. Fig. 6a shows the clock frequency shifting signal used in the simulated data generator (upper trace) and the recovered VCO frequency shifting signal at the conventional clock recovery circuit. Fig. 6b shows the same for the modified clock recovery circuit with NLA. It can be observed that the amplitude of the recovered shifting signal (lower trace) is more in the proposed system than that in the conventional system. Also the time rate of change of the control voltage at the shifting instants per unit control voltage for these two systems are different. For conventional system it is 1.2987 m s^{-1} and for the proposed system 2.0408 m s^{-1}. This means that the proposed system has not faster transient response and the design parameters used in the laboratory experiment, the enhancement in speed is more than 50%.

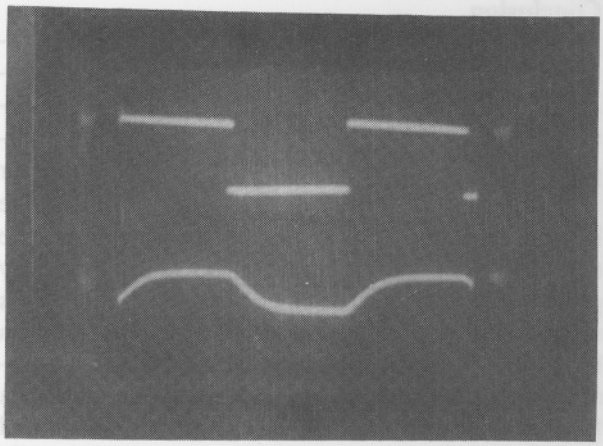

Fig. 6a—Photograph of the oscilloscope traces in the experiment with the conventional system; upper trace: modulating signal used to generate FSK-type data clock; lower-trace: demodulated signal at the loop VCO control end

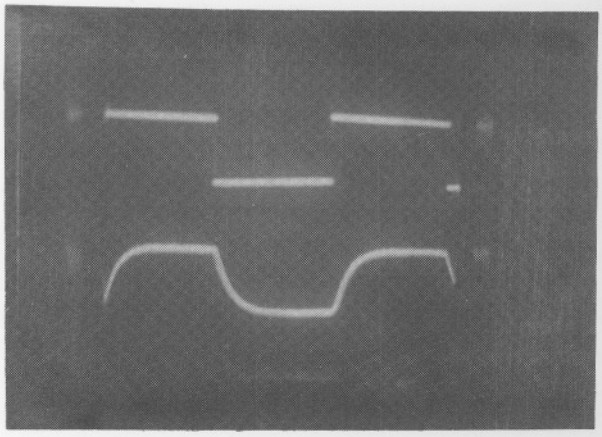

Fig. 6b—Photograph of the oscilloscope traces in the experiment with the proposed modified system; upper trace; modulating signal used to generate FSK-type data clock; lower trace: demodulated signal at the loop VCO control input

Conclusion

These investigations show that the transient response speed and the acquisition range of the proposed circuit are more than those of the conventional circuits without NLA. The performance improvement depends on the NLA design parameter in a complicated way. For the system used in the laboratory experiment, the enhancement in the transient response is found to be more than fifty per cent. Intutive arguments indicate that there is no problem regarding the stability of the loop as long as the design parameter of the NLA is resonably small and there is no additional time delay in the NLA; when the NLA introduces additional time delay, the system would become conditionally stable. Further for a practical op-amp and diode based NLA, the output of the NLA would be limited when its input crosses a design-dependent value and thus the cubic model of the non-linearity would not hold good.

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