High input impedance first-order allpass, highpass and lowpass filters with grounded capacitor using single DVCC

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Received 5 January 2010; accepted 4 May 2010

A voltage-mode high input impedance first-order allpass, highpass and lowpass filters using one differential voltage current conveyor (DVCC), one grounded capacitor and two resistors is presented. The allpass, highpass and lowpass signals can be obtained simultaneously from the circuit configuration. The simulation results confirm the theoretical analysis.

Keywords: Current conveyor, First-order, Allpass filter, Analog signal processing

Current conveyors (CCs) and current feedback amplifiers (CFAs) are receiving much attention for their potential advantages such as inherent wider signal bandwidths, simpler circuitry and larger dynamic range. Considering these advantages of CCs and CFAs, several current and voltage-mode first-order allpass filters using various active components have been reported. This paper proposes a new voltage-mode first-order allpass, highpass and lowpass filters.

Voltage-mode active filters with high input impedance are of great interest because they can be directly connected in cascade to implement higher order filters. On the other hand, the use of only grounded capacitor is beneficial from the point of view of integrated circuit fabrications. Several voltage-mode first-order allpass filters using various active components have been reported. Some circuits use two active components to realize such a first-order allpass filter function. However, the active components they used are not canonical. Some circuits use one active component and three or more passive components. However, the capacitors they used are not grounded. Some circuits use one second-generation current conveyor (CCII), one grounded capacitor and two or three resistors. However, these circuits have not the advantage of high input impedance. Several researchers proposed a voltage-mode first-order allpass filter using one differential difference current conveyor (DDCC), one capacitor and one resistor. However, these circuits still have not the advantage of high input impedance. Metin and Cicekoglu proposed a first-order allpass filter with high input impedance using one modified CCII, two resistors and one grounded capacitor. Biolek and Biolkova proposed a first-order allpass filter with high input impedance using one voltage differencing-differential input buffered amplifier and one grounded capacitor.

In this paper, a new voltage-mode first-order allpass, highpass and lowpass filters using one differential voltage current conveyor (DVCC), one grounded capacitor and two resistors is presented. The proposed circuit has the advantage of high input impedance. With respect to the previous first-order allpass filters, the proposed circuit employs only one active component, grounded capacitor and has the advantage of high input impedance, and two more filter types (highpass and lowpass) can be simultaneously obtained from the circuit configuration.

The Proposed Circuit

The DVCC can be characterized by

\[
\begin{bmatrix}
i_{y1} \\
i_{y2} \\
v_x \\
i_z
\end{bmatrix} =
\begin{bmatrix}
0 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 \\
1 & -1 & 0 & 0 \\
0 & 0 & \pm 1 & 0
\end{bmatrix}
\begin{bmatrix}
v_{y1} \\
v_{y2} \\
i_x \\
i_z
\end{bmatrix}
\]

\[\ldots (1)\]

The CMOS implementation of DVCC is shown in Fig. 1, which is obtained from Fig. 5 of Elwan and

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The multiple current outputs can be easily implemented by adding output branches. The proposed voltage-mode first-order allpass, highpass and lowpass filters using one DVCC, one grounded capacitor and two resistors is shown in Fig. 2. The voltage transfer functions can be expressed as

\[ V_{o1} = \frac{sC}{sC + G_1} \quad \ldots \quad (2) \]

\[ V_{o2} = \frac{G_1}{sC + G_1} \quad \ldots \quad (3) \]

\[ V_{o3} = -\frac{sC R_2 + G_1}{sC} \quad \ldots \quad (4) \]

From Eqs (2)-(4) it can be seen that a first-order highpass response is obtained from \( V_{o1} \), a first-order lowpass response is obtained from \( V_{o2} \), and if \( R_2 = R_1 \), a first-order allpass response is obtained from \( V_{o3} \). Because the input terminal of the proposed first-order allpass filter is connected directly to the \( y_1 \) terminal of the DVCC, the input terminal has the advantage of high input impedance.

**Sensitivities Analysis**

Taking into consideration the DVCC non-idealities, the port relations in Eq. (1) can be expressed as

\[ v_x = \beta_1v_{y_1} - \beta_2v_{y_2} \quad \text{and} \quad i_{zk} = \pm\alpha_ki_x \quad \ldots \quad (5) \]

where \( \beta_j = 1 - \epsilon_{yj} \) and \( \alpha_k = 1 - \epsilon_{ik} \) for \( j = 1, 2 \) and \( k = 1, 2, 3 \). Here \( \epsilon_{yj} (|\epsilon_{yj}|<<1) \) denotes the voltage tracking errors of the DVCC and \( \epsilon_{ik} (|\epsilon_{ik}|<<1) \) denotes the current tracking error from the \( x \) terminal to the \( k \)th \( z \) terminal of the DVCC. Reanalysis of the filter circuit in Fig. 2 yields the following modified transfer function of \( V_{o2} \):

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Table I–TSMC SPICE parameters for level 3, 0.35 μm CMOS process

<table>
<thead>
<tr>
<th>Parameters</th>
<th>NMOS PARAMETERS</th>
</tr>
</thead>
<tbody>
<tr>
<td>.MODEL MbreakN NMOS (LEVEL=3 TOX=7.9E-9 NSUB=1E17</td>
<td>+ GAMMA=0.5827871 PHI=0.7 VTO=0.5445549 DELTA=0</td>
</tr>
<tr>
<td>+ UO=436.256147 ETA=0 THETA=0.1749684 KP=2.055786E-4</td>
<td>+ VMAX=8.309444E4 KAPPA=0.2574081 RSH=0.0559398</td>
</tr>
<tr>
<td>+ NFS=1E12 TPG=1 JI=3E-7 LD=3.162278E-11 WD=7.046724E-8</td>
<td>+ CGDO=2.82E-10 CGSO=2.82E-10 CGBO=1E-10 CJ=1E-3</td>
</tr>
<tr>
<td>+ PB=0.97558533 MJ=0.3448504 CJSW=3.777852E-10</td>
<td>+ MJSW=0.3508721</td>
</tr>
</tbody>
</table>

| .MODEL MbreakP PMOS (LEVEL=3 TOX=7.9E-9 NSUB=1E17 | + GAMMA=0.4083894 PHI=0.7 VTO=0.7140674 DELTA=0 |
| + UO=212.2319801 ETA=9.999762E-4 THETA=0.2020774 | + KP=6.733755E-5 VMAX=1.181551E5 KAPPA=1.5 |
| + RSH=30.0712458 NFS=1E12 TPG=1 JI=2E-7 LD=5.000001E-13 | + RW=1.249872E-7 CGDO=3.09E-10 CGSO=3.09E-10 |
| + WD=5.000001E-13 | + CGBO=1E-10 CJ=1.419508E-3 PB=0.8152753 MJ=0.5 |
| + PB=0.97558533 MJ=0.3448504 CJSW=3.777852E-10 | + MJSW=0.3508721 |
The cutoff frequency is obtained by
\[ \omega_c = \frac{\beta_1 (\alpha_1 + \alpha_2 - \alpha_3)}{CR_1} \quad \ldots (7) \]

The active and passive sensitivities are low and obtained as
\[ S_{\alpha_i}^{\omega} = \frac{\alpha_i}{\alpha_1 + \alpha_2 - \alpha_3} ; \]
\[ S_{\beta_2}^{\omega} = 1 \]

Simulation Results

The first-order filters in Fig. 2 were simulated using HSPICE. The DVCC was realized by the CMOS implementation in Fig. 1 whereas the aspect ratios of the NMOS and PMOS transistors are \( W/L = 3.5 \mu \text{m}/0.7 \mu \text{m} \) and \( W/L = 7 \mu \text{m}/0.7 \mu \text{m} \), respectively, using \( 0.35 \mu \text{m} \) MOSFET from TSMC (the model parameters are given in Table 1). Figures 3(a), (b) and (c) represent the magnitude and phase responses of the first-order highpass, lowpass and allpass responses, respectively, designed with \( f_c = 1.59 \text{ MHz} \): \( C = 10 \text{ pF} \) and \( R_1 = R_2 = 10 \text{ k}\Omega \). The power supply was \( \pm 1.65 \text{ V} \). The bias voltages are \( V_{b1} = -0.25 \text{ V} \) and \( V_{b2} = 0.5 \text{ V} \).

Conclusions

A new voltage-mode first-order filter configuration using one DVCC, one grounded capacitor and two resistors is presented. The allpass, highpass and lowpass filters can be simultaneously obtained from the same circuit configuration. The proposed circuit has the advantage of high input impedance. The simulation results confirm the theoretical analysis.

Acknowledgment

The authors would like to thank the anonymous reviewers for their constructive criticisms to improve the manuscript.

References