Modeling power VDMOSFET transistors: Device physics and equivalent circuit model with parameter extraction

Rakesh Vaid & Naresh Padha
Department of Physics and Electronics, University of Jammu, Jammu 180 006
and
Anil Kumar & R S Gupta
Semiconductor Device Research Laboratory, Department of Electronic Science,
University of Delhi, South Campus, New Delhi 110 021
and
Chetan D Parikh
Motorola, Inc. MD-K10, 3501 Ed Bluestein Blvd. Austin, TX 78721, USA

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A power VDMOSFET has been simulated using PISCES-II, a 2-D numerical device simulator. The doping densities and device dimensions are chosen so as to simulate a typical device structure with one micron channel length. These simulations are aimed at understanding the device physics through various internal electrical quantities like potential distribution, electric field distribution, and electron concentrations etc. in different regions of the device both in on/off states. Simulated results have been used to extract circuit model parameters like $V_T$, $K_P$ and $\lambda$ etc. for a VDMOSFET equivalent circuit model comprising of a lateral MOSFET in series with a JFET. It advances the earlier models in terms of number of parameters extracted for its SPICE implementation. The characteristics obtained from the dc circuit model show good agreement with the simulated data, thus validating the device operation, the circuit model and its parameter extraction procedures.

[Keywords: Power MOSFET, VDMOSFET, Device simulation, Parameter extraction]

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1 Introduction

The field of power devices is of growing interest in recent years. Voltage, current and power handling capabilities of power semiconductor devices have grown steadily leading to new applications. Metal oxide semiconductor (MOS) devices have been widely used for over two decades in low power and very large scale integration (VLSI) circuit applications. In the last few years, MOS transistors rated for high power level have been developed. These devices have several advantages over bipolar in power circuits. The MOSFETs for power applications cannot be fabricated by merely scaling up low-power MOSFETs to the desired voltage and current. The high voltage blocking ability requires a large depletion area across the reverse-biased P-N (body/drift) junction of the VDMOSFET (vertical double-diffused MOSFET). Thus, the power VDMOSFET structure contains a low-doped epi-layer in series with the drain region of the transistor in order to increase the drain-source breakdown voltage. Furthermore, it increases the current densities by providing vertical current flow lines1,2.

Several models for VDMOSFET transistors have been described in the literature3-14 based on various aspects of the modelling. Earlier papers addressed specific aspects, such as breakdown voltage and on resistance modelling3-5 which calculate the various resistances assuming constant current densities in the various regions and hence derive equations in terms of the geometrical parameters of the device.
Subsequently, complete analytical dc models for the power MOSFET were reported which include complete details of quasi-saturation effect. Kim and Fossum\(^6\) presented a model which included the non-uniform doping density in the channel region, field dependence of mobility, the two-dimensional current flow through the accumulation region, quasi-saturation in the JFET region, the current spread in the drift region, and the parasitic bipolar transistor. Tsai \textit{et al.}\(^7\) improved this model taking reverse biased conditions by modelling the built-in parasitic BJT and transients for all charge regions of the device. Their drawback is that it is mathematically complex, and requires the solution of coupled transcendental equations; and is difficult to implement into a circuit simulator. The model by Scott and Franz\(^8\) focused on the three inter-electrode capacitances, but it lacks a physical steady-state model, which is the basis of accurate transient simulations. Attempts to model power MOSFETs have been complicated by the existence of the lightly doped drain present in high voltage devices. This lightly doped region can greatly affect the on resistance, saturation current, and feedback capacitance of the device.

Equivalent circuit models are the most popular with the circuit designers, as they represent the power MOSFET as an equivalent circuit that can directly be used in circuit simulators. These models use standard circuit elements for their equivalent circuit representation. Various such models have been proposed\(^9\)–\(^14\). Their primary disadvantage is that it is not easy to extract all the parameters associated with such models. Thus, the most desirable feature of an equivalent circuit simulation model should be its simplicity and ease with which the model parameters could be extracted. The total number of components that constitute the model must be kept to a minimum to improve the simulation efficiency of complex systems. The model validity can be enhanced if its components can be associated with the physical principles of the device operation. This feature is particularly important in semiconductor devices because in addition to predicting system performance, models are used to estimate the sensitivity of a system to semiconductor process and device parameter variations especially in a manufacturing environment.

In this paper, a simple equivalent circuit model of power VDMOSFET transistor suitable for circuit simulation is used to model the device operation. The model parameters are extracted from the terminal characteristics of the device structure simulated using PISCES-II (Ref. 15). Complete parameter extraction procedures are presented. The model is based on the physical principles of the VDMOSFET device operation\(^8,9\) and it advances the prior efforts\(^9,11,12\) in accurately predicting the circuit model parameters based on device simulation results. This paper explains the complete parameter extraction procedures for VDMOSFET equivalent circuit model comprising of a lateral MOSFET in series with a JFET and a drain resistance. In JFET part of the parameter extraction procedures, a new approach has been used to find the model parameters. It is shown that if the parameter $\beta$ of the JFET is made equal to $K_P$ of the lateral MOSFET, circuit model gives the best results. A circuit simulation program PSPICE has been used to implement the circuit model and verify with the detailed data obtained from PISCES-II.

### 2 Device Operation and Simulations

As shown in Fig. 1, a VDMOSFET is different from a low power MOSFET in the following aspects:

![Schematic design of a VDMOSFET transistor. Structure shown represents “half-cell” of the device. All dimensions are as indicated in Table 1](image-url)
(i) the source and drain (drift region) are not symmetric; (ii) there is a long vertical, low-doped drift region which enables the device to block high voltage; (iii) the gate overlaps both the channel and the drift region, so that an accumulation layer is formed in the linear operating region to enhance the conductivity (the accumulation layer is replaced by a depletion layer at high $V_{ds}$); (iv) the source contact overlaps the P-body region to short-circuit the source/body junction, ensuring that the parasitic BJT is normally off and (v) the channel region has graded doping. A typical n-channel VDMOSFET simulated using PISCES-II has been used and these simulations provide new insights both in on/off state, which facilitate the device modelling for circuit simulation. The model has been restricted to the dc characteristics only. The device simulations take into account the mobility model that is dependent on impurity concentration and impact ionization at a temperature of 300 degree Kelvin. The geometrical dimensions along with the doping densities used for the device simulations are listed in Table 1.

### 2.1 VDMOSFET in off state

The off state ($V_{gs}<V_T$) behaviour of the device is studied by the various simulation results. Fig. 2 shows the electron concentration plot in the drift region for lower values of the drain voltage and shows that the electron concentration is higher at the surface i.e. accumulation. With increasing $V_{ds}$, the electron concentration decreases at the surface and remains constant far away from the surface in accordance with the device operation. Fig. 3 shows the electric field variations at the device surface. Since the N+/P junction is at a fixed potential, the change in the electric field with $V_{ds}$ is mainly in the drift region. One thing is clear that as long as $V_{ds} < V_{gs}$ the electric field is less in the drift region as compared to the initial electric field (when $V_{gs} = 1$V and $V_{ds} = 0$V). Similar approach is applicable at the channel surface and the variation is only at the P-body and drift region junction.

Potential variations shown in Fig. 4 are non-linear at the surface in the channel region due to the non-uniform doping in this region. It is further observed that left junction (N+/P) remains at its junction

| Table 1 — Design parameters used for VDMOSFET simulation |
|----------------|------------------|
| Parameter     | Value            |
| L_{Acc}       | 2.3 μm           |
| L_{ch}        | 1.0 μm           |
| L_{T}         | 5.0 μm           |
| W_{T}         | 4.0 μm           |
| t_{ox}        | 0.1 μm           |
| d_{p}         | 1.2 μm           |
| L_{n+}        | 0.5 μm           |
| d_{n+}        | 0.2 μm           |
| N_{n-}        | $5.0 \times 10^{15}$ cm$^{-3}$ |
| N_{n+}        | $5.0 \times 10^{19}$ cm$^{-3}$ |
| N_{p}         | $1.0 \times 10^{17}$ cm$^{-3}$ |
potential only, since (N'/P) are connected to the
ground and there is a rise in the potential near the
right junction (P/N') with the increase in the drain
voltage. Depletion region advancements with the
increasing drain voltages are shown in Fig. 5, indicate
that depletion region penetrates more and more in the
lightly doped N-region which is desired. A key
observation is that as long as the drain voltage is less
than the gate voltage, the depletion region is
negligible at the surface of the drift region since it is
the rich area of electrons (accumulation). As the drain

2.2 VDMOSFET in on state

The VDMOSFET in on state means $V_{gs} > V_T$. Fig. 6
shows the electron concentration variations in the
channel region and shows that the device is the
inverted mode at the channel surface. As we move
away from the surface the electron concentration
decreases in the P-body region (channel) due to the
non-uniform doping in this area and becomes constant
beyond a certain position. Electric field distribution,
shown in Fig. 7 indicates that only the magnitude is
different whereas the basic principle of variation
remains the same as discussed in the off state. The
observation here is that the electric field varies in

![Graph](image1)

**Fig. 4** — Potential variations at the channel surface for various $V_{ds}$ values in off state

![Graph](image2)

**Fig. 5** — Depletion region edge advancements with the increasing drain voltage in the off state. The axes correspond to those shown in Fig. 1

![Graph](image3)

**Fig. 6** — Electron concentration variations in the channel region in on state at $x = 1.5 \mu m (V_{gs} > V_T)$

![Graph](image4)

**Fig. 7** — Electric field variations along the channel surface with increasing drain bias in on state ($V_{gs} > V_T$)
negative direction till the large value of the drain voltage. Also it is observed that the electric field is non-uniform in the channel region because of the doping profile. Fig. 8 shows the potential variations at the surface and in the channel region. It is observed that the potential in the drift region increases with the increase in drain voltage and the magnitude of this potential is higher as compared to the magnitude in the off state. Since the device is in on state the potential variation at the channel surface is increasing from left to right due to the fact that doping is in the exact opposite manner and hence the electric field is higher on the right side of the channel surface. The device has been operated over a wide range of \( V_{ds} \)/\( V_{gs} \) values in on/off state to obtain the I-V characteristics and the simulations reveal that the device works well over the entire range of voltages.

3. Circuit Modelling and Parameter Extraction

Numerous circuit models for the power VDMOSFET have been reported in the literature\(^8\)\(^-\)\(^14\) and tried to extract the basic parameters required for its implementation with a SPICE like circuit simulator such as PSPICE. The circuit model used for simulation is shown in Fig. 9. It is a simple circuit model consisting of a SPICE level 1 MOSFET, a JFET as the basic elements and a series drain resistance (\( R_D \)). VDMOSFET structure can be now understood in terms of a vertical JFET driven in cascade from a lateral low voltage MOSFET. When the gate is positively biased with respect to the source, an accumulation layer exists in the N' region beneath the gate. This accumulation layer acts as drain of the lateral MOSFET and the source of the vertical JFET.

The JFET channel is the region between the two P-body diffusions, which act as the gate of the JFET. The JFET drain is the N' bulk usually thought of as the power MOSFET drain.

3.1 MOSFET parameter extraction

SPICE level 1 MOSFET model is chosen to represent the lateral MOSFET. The level 1 MOSFET model mainly requires three parameters namely \( V_T \), \( K_P \) and \( \lambda \) for its SPICE implementation. To find the \( V_T \) and \( K_P \) of MOSFET, equation of the MOS transistor\(^16\) in the triode region is used i.e.

\[
I_{ds} = \mu_n C_{ox} \frac{W}{L} (V_{gs} - V_T - 0.5V_{ds}) \frac{V_{ds}}{V_{ds}} \quad \text{(1)}
\]

From this it is seen that \( V_T = \text{intercept} - 0.5V_{ds} \).

For \( L = W = 1 \mu m \) (since \( L_{ch} = 1 \mu m \) and PISCES assumes \( W = 1 \mu m \)), \( \mu_n C_{ox} = K_P \) and ignoring \( V_{ds} \) in Eq. 1 we get,

\[
I_{ds} \cong K_P (V_{gs} - V_T) V_{ds} \quad \text{(2)}
\]

Which gives \( K_P = \text{slope/}V_{ds} \).

The values found at \( V_{ds} = 0.1 \text{ V} \) are \( V_T = 4.11 \text{ V} \) and \( K_P = 13.1 \times 10^{-6} \text{ A/V}^2 \).

Now for a verification purpose we calculated \( V_T \) and \( K_P \) values from the high order curve at \( V_{ds} = 20 \text{V} \) and the equation of the MOS transistor\(^16\) in the saturation region is used i.e.
$I_{ds} = \frac{K_p}{2} (V_{gs} - V_T)^2 \quad \ldots (3)$

It is seen that, $V_T =$ Intercept and $\sqrt{\frac{K_p}{2}} =$ Slope.

The values found using this method are

$V_T = 4.096 \text{ V}$ and $K_p = 17.17 \times 10^{-6} \text{ A/V}^2$.

It is observed that more or less same values for $V_T$ and $K_p$ are obtained with this method also. Therefore, the values of $V_T$ and $K_p$ are selected as obtained from the low $V_{ds}$ curve.

3.2 Determination of Lambda ($\lambda$)

The $\lambda$ is a saturation region parameter and can be determined from the slope of the $I_{ds}-V_{ds}$ curve in the saturation region ($V_{ds} > V_{dssat}$) by dividing the slope value by the Y-intercept$^{17}$. Another method$^{18}$ relates the average conductance for $V_{ds} > V_{dssat}$ as

$G_{dssat} = I_{dssat} \frac{\lambda}{(1 - \lambda V_{ds})^2} \quad \ldots (4)$

The value of $\lambda$ can be calculated approximately by neglecting the term $\lambda V_{ds}$ from the above equation. Hence, $\lambda = G_{dssat} / I_{dssat}$. The extracted value of $\lambda = 0.018 \text{ V}^{-1}$.

3.3 Determination of drain resistance ($R_D$)

The drain resistance used in circuit model is calculated from the $I_{ds}-V_{gs}$ curve for a lower $V_{ds}$ value ($V_{ds} = 0.1 \text{ V}$) in the linear region. It is observed that as $V_{gs}$ increases, $R_D$ decreases and then tends to saturate towards a constant value as shown in Fig. 10. The $R_D$ value found using this method is equal to 21.2 k$\Omega$.

3.4 JFET parameter extraction

For the implementation of the JFET part of the circuit model in PSPICE, two parameters $V_T$ and $\beta$ are required. In JFET, the current prior to pinch off is given by$^{19}$

$I_{ds} = \beta V_{ds} (2 (V_{gs} - V_T) - V_{ds}) \quad \ldots (5)$

where $V_T = -V_P$, $V_P$ being the pinch-off voltage. For $V_{gs} = 0 \text{ V}$ and defining, resistance $R = V_{ds} / I_{ds}$, we get

$\frac{1}{R} = \beta (2 V_P - V_{ds}) \quad \ldots (6)$

Note, for the JFET, drain is the same as drain of the VDMOSFET transistor and source corresponds to the drain of the lateral MOSFET. VDMOSFET source acts like the gate of the JFET. If the gate bias of the VDMOSFET is high, the resistance of the MOSFET channel is small and it may be assumed that the entire $V_{ds}$ of the VDMOSFET transistor appears as $V_{ds}$ of the JFET. Thus, if $V_{gs}$ of the VDMOSFET transistor is made large (assuming the source to be grounded) it would ensure that $V_{ds} \approx V_{dssat}$ and $V_{gs} \approx 0 \text{ V}$ for the JFET. The plot of $1/R$ vs. $V_{ds}$ using Eq. (6) would yield parameters $V_P$ and $\beta$ of the JFET. Fig. 11 shows the variation of $I_{ds} / V_{ds} $ with $V_{ds}$ for large gate bias ($V_{gs} = 12 \text{ V}$). A straight-line fit is also shown in Fig. 11. From this figure, $V_P$ and $\beta$ of JFET are found as $V_P = 25.9 \text{ V}$ and $\beta = 7.125 \times 10^{-7} \text{ A/V}^2$.

3.5 Model implementation

With the circuit parameters obtained above, the model is implemented using PSPICE. I-V characteristics obtained from the circuit model are compared with those obtained from PISCES. The agreement between the results is not satisfactory. The

![Fig. 10 — $I_{ds}-V_{ds}$ characteristics of the model with ($\beta = K_P$) along with the PISCES results](image)

![Fig. 11 — Equivalent circuit model of VDMOSFET transistor](image)
discrepancy may be due to the fact that JFET parameters are extracted assuming its $V_{gs} \cong 0V$, which is practically not true, because some definite voltage drop takes place across the MOSFET channel. Since it is difficult to calculate this voltage drop, the assumption ($V_{gs} \cong 0V$) has to be used in calculations. Here it is observed that the extracted value of $\beta$ is not sufficient to ON the JFET. If $\beta$ of the JFET is made equal to the $K_p$ of the lateral MOSFET, it is found that this value of $\beta$ is sufficient to ON the JFET, which was also suggested by Perugupalli et al.\textsuperscript{20} and is therefore considered in the present analysis. Implementing $\beta = K_p$ for JFET, the I-V characteristics of circuit model are again compared with the PISCES results. An excellent fit is obtained over a wide range of $V_{ds}$ and $V_{gs}$ values as shown in Figs. 12 and 13. Hence it is proposed to use $\beta = K_p$ for the JFET in the circuit model. The proposed model behaves in accordance with various physical models reported in the literature\textsuperscript{6-7} and is clearly very attractive from circuit simulation point of view, as it can be implemented as a simple SPICE sub circuit. Any of the SPICE like circuit simulators can be used due to their universal availability. Furthermore, the parameter extraction procedures are quite simple and systematic.

4 Conclusion

Power VDMOSFET device operation has been discussed both in on/off states with the help of various internal electrical quantities such as electron concentration; potential distribution etc. based on the device simulation results obtained using PISCES-II. An equivalent circuit model for the power VDMOSFET suitable for use with the SPICE like circuit simulators has been presented. It accurately predicts the static characteristics of a power VDMOSFET. The model parameters are easy to determine from the terminal characteristics of the device. Complete parameter extraction techniques are presented. The model gives an excellent fit with those of the simulated data in the dc regimes. However a similar approach could be followed to analyse the complete small-signal behaviour of the device to give its complete small signal model. Parameter extraction methods may be modified for modelling other power devices such as LDMOSFET and CMOS compatible LDMOSFET. Furthermore, these results may be very useful for the circuit designers to incorporate VDMOSFET in their circuit analysis without having any standard VDMOSFET model.

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