Effect of grain size on the mobility and transfer characteristics of polysilicon thin-film transistors

Navneet Gupta* & B P Tyagi**

*Department of Physics, Graphic Era Institute of Technology, Dehradun, Uttaranchal
**Department of Physics, D. B. S (Post Graduate) College, Dehradun, Uttaranchal

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The effect of the grain size on the effective carrier mobility ($\mu_{\text{eff}}$) and transfer characteristics of a polycrystalline silicon thin-film transistor (poly-Si TFT) have been theoretically investigated by developing an analytical model. The dependence of $\mu_{\text{eff}}$ is studied as a function of doping concentrations and gate voltage for different values of grain size. It is observed that at low as well as at high doping concentrations, the effective carrier mobility ($\mu_{\text{eff}}$) increases with increase in grain size, whereas the observed dip at the intermediate doping concentration is getting confirmed. The effect of the grain size on transfer characteristics of poly-Si TFT in its linear region is also presented. It is found that at low gate voltages, $\mu_{\text{eff}}$ and $I_D$ increase rapidly with the increase in $V_G$ for all values of grain sizes due to the grain boundary barrier lowering effect. At high gate voltage the grain boundary barrier lowering effect becomes insignificant and causes the saturation of $\mu_{\text{eff}}$ and $I_D$. The model was found to account correctly for the experimentally observed mobility variation and yield a reasonably good agreement.

[Keywords: Mobility, Polysilicon thin-film transistors, Grain size]

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1 Introduction

Technologically, polycrystalline silicon thin-film transistors (poly-Si TFTs) have gained tremendous importance because these are key devices in large area electronics applications, including active-matrix liquid crystal displays (AMLCDs) and solid-state image sensors$^{1,2}$. The polysilicon material used in the channel of thin-film transistors is composed of a linear chain of silicon crystallites (grains) separated by the regions with high density of impurities called grain boundaries (GBs). The GBs, although physically much smaller than the individual grains, greatly influence the conduction properties of the material. By the presence of GBs in the channel, the performance of poly-Si TFT is degraded$^{3,4}$. These GBs present in the channel are mainly responsible for the scattering of majority carriers, this in turn create a potential barrier which restricts the flow of charge carriers from grain to grain. The effects of GBs can be reduced either by passivating the boundary trap states in the film$^{5,6}$ or by increasing the grain size and thus reducing the number of grain boundaries present in the active channel of the TFT device$^{7,8}$. In the present model it is considered that there are $n_g$ number of grains separated by $(n_g-1)$ number of GBs in the channel. When poly-Si film is doped with one type of impurity, most dopants enter the crystallite lattice substitutionally and are uniformly distributed throughout the film with a concentration of $N$ (cm$^{-3}$). To simplify the model it is assumed that:

1. Poly-Si film in the channel of TFT is composed of identical grains; 
2. GBs are straight and perpendicular to the carrier flow in the channel and are of negligible thickness compared to grains; 
3. It contains $N_T$ (cm$^{-2}$) number of traps located at energy $E_T$ with respect to the intrinsic Fermi level; 
4. Thermionic emission of electrons over the potential barrier ($\psi_B$) is considered to be the dominant current mechanism at room temperature.

The model accounts for the effects of grain size ($D_G$) on poly-Si mobility and drain current in a poly-Si TFT as a function of doping concentration ($N$) and gate voltage ($V_G$), in the linear region ($V_D = 0.1$ V) of the poly-Si TFT characteristics. The calculated values are compared with the experimental variations and a reasonably good agreement is observed.
2 Theory

The crystal structure of a typical grain and energy band diagram of the channel of a polycrystalline silicon thin film transistor (poly-Si TFT), considered for analysis, is shown in Fig. 1 (a and b). The channel of a poly-Si TFT is assumed to be made up of identical grains of size $D_G$ separated by GBs of thickness $D_{GB}$ having a density of trapping states $N_T$ located at an energy $E_T$. The traps are assumed to be initially neutral and become charged by trapping carriers, thereby creating a space charge (depletion) region and hence create potential barriers on both sides of the GBs. Let $D_d$ is the width depletion region on one side of the grain boundary.

The free carriers are captured at a certain rate by the GB traps which become charged, and at the same time the carriers are also released from the filled trap states at a certain rate, and finally equilibrium is reached. The trapping states density ($N_T$) is found to decrease with increasing grain size ($D_G$) which may be attributed to a decrease in disorder in larger grains. To incorporate this effect, an empirical relation between $N_T$ and $D_G$ which fits with the experimentally available value is given by:\[ N_T = (35 + 2.55 D_G^{0.363}) \times 10^{10} \text{ (cm}^{-2}) \] ...

Although polysilicon is a three-dimensional material, for the purpose of calculating its transport properties, it is sufficient to treat the problem in one dimension. Using the above approximation, Poisson's equation becomes:

$$d^2V/dx^2 = qN/\varepsilon_s$$

when, \((D_G-2D_d)/2 \leq |x| \leq D_G/2\) ...

where $\varepsilon_s$ is the dielectric permittivity of polysilicon.

Integrating Eq. (2) twice and applying the boundary conditions that $V(x)$ is continuous and $dV/dx = 0$ at $x = (D_G-2D_d)/2$ gives:

$$V(x) = (qN/2\varepsilon_s)x^2 + V_o \quad |x| \leq D_G/2$$

where $V_o$ is the potential of the valence band edge at the centre of the crystallite. In this model we have assumed the intrinsic fermi level to be zero for calculation and energy is positive towards the valence band. Now for a given crystallite size, there are two cases: (i) fully depleted grains and traps are partially filled and (ii) partially depleted grains.

In first case, the crystallites are completely depleted of carriers and the traps are partially filled, so that \((D_G-2D_d)/2 = 0\) and Eq. (2) becomes:

$$V(x) = (qN/2\varepsilon_s)x^2 + V_o \quad |x| \leq D_G/2$$ ...

The potential barrier height ($\psi_B$) is given by:

$$\psi_B = V(D_G/2) - V(0)$$

$$\psi_B = q D_G^2 N/8\varepsilon_s$$ ... (5)

In second case, only part of crystallites is depleted of carriers and $\psi_B = V((D_G-2D_d)/2)$ > 0. The potential barrier height ($\psi_B$) is given by:

$$\psi_B = V(D_G/2) - V((D_G-2D_d)/2)$$

At critical doping concentration $N^* \approx N_T/D_G$

$$\psi_B = q N_T^2 /8N\varepsilon_s$$ ...

The height $\psi_B$ of the potential barrier which exists at the grain boundary in an idealized poly-Si film (with average grain size $D_G$ and grain boundary trap-state density $N_T$) is given by Eq. (5) if the doping concentration $N < N^*$ and by Eq. (6) if $N > N^*$. 

![Model for (a) crystal structure and (b) energy band diagram of the channel of a poly-Si TFT](image-url)
Now considering grain and GBs as series resistances in the channel of a poly-Si TFT, the total channel resistance \( R_T \) can be written as:

\[
R_T = n_g R_G + (n_g-1) R_{GB}
\]  \( \ldots (7) \)

\[
D/\mu_{eff} = n_g D_G/\mu_G + (n_g-1)D_{GB}/\mu_{GB} \exp[-q\psi_B/kT]
\]

Hence the effective carrier mobility of a poly-Si TFT is given by:\(^{10}\):

\[
\mu_{eff} = \mu_G/1 + [(n_g-1)\mu_GD_{GB}/n_g\mu_{GB}D_G] \exp[q\psi_B/kT] \ldots (8)
\]

The drain current for the output characteristic of a poly-Si TFT is given by:

\[
I_D = (\mu_{eff} ZC_{ox}/D) [(V_G - V_T)V_D - V_D^2/2] \ldots (9)
\]

where, \( C_{ox} = \varepsilon_{ox}/t_{ox} \) (where \( \varepsilon_{ox} \) is dielectric permittivity of oxide film and \( t_{ox} \) is the thickness of oxide film) is the gate oxide capacitance per unit area, \( V_T \) is threshold voltage and \( Z \) is channel width.

In the linear region where \( V_D << (V_G - V_T) \), hence from Eqs (8) and (9) we get:

\[
I_D = \{1 + [(n_g-1)\mu_GD_{GB}/n_g\mu_{GB}D_G] \exp[q\psi_B/kT]\}^{1+}(V_G - V_T)V_D/2
\]

The values of potential barrier height (\( \psi_B \)) for a poly-Si TFT at room temperature, assuming mono-energetic traps at the grain boundaries, in the term of gate voltage is given by the relation:\(^{11}\):

\[
\psi_B = q^2 N_t^2 t_{si}/8\varepsilon_{ox}(V_G - V_T) \ldots (10)
\]

where \( t_{si} \) is the polysilicon film thickness.

3 Discussion

The effect of grain size on the effective carrier mobility and transfer characteristics of poly-Si TFT have been studied. The effective carrier mobility (\( \mu_{eff} \)) is computed for different values of grain size (50 to 1000nm) as a function of both doping concentration and gate voltage at room temperature, considering the conduction to be due to thermionic emission. The parameters taken for calculation for a poly-Si TFT\(^{12}\) are \( \mu_G = 203 \text{ cm}^2\text{V}^{-1}\text{sec}^{-1} \), \( \mu_{GB} = 0.3 \text{ cm}^2\text{V}^{-1}\text{sec}^{-1} \), \( D = 10 \mu\text{m} \), \( Z = 10 \mu\text{m} \), \( D_{GB} = 2 \text{nm} \), \( V_D = 0.1 \text{ V} \), \( V_T = 2.45 \text{ V} \), \( t_s = 4 \text{ nm} \), \( t_{ox} = 100 \text{ nm} \) and \( C_{ox} = 354 \mu\text{Fm}^{-2} \). The computed variations of effective carrier mobility (\( \mu_{eff} \)) with doping concentration for different grain sizes, that is for different number of grains in the channel is shown in Fig. 2.

At low as well as high doping concentration the effective carrier mobility (\( \mu_{eff} \)) increases with increase in grain size and hence with decrease in number of grains. This confirms the observed dip at the intermediate doping concentration\(^{13}\). The mobility is initially high at low doping concentration because grains are fully depleted and traps are partially filled and the potential barriers at the GBs have not been formed. As doping concentration is increased, potential barrier develops and mobility is decreased, reaching a minimum when barrier height is maximum. This mobility dip occurs at a critical doping concentration (\( N^* \)), at which all traps at the grain boundaries are filled with carriers. There exists a mobility minimum for each value of grain size (\( D_G \)). The mobility minimum is found to shift towards lower \( N \) as grain size is increased. For any value of \( D_G \) the position of the effective carrier mobility (\( \mu_{eff} \)) minimum depends on the choice of the parameters, particularly the grain boundary width (\( D_{GB} \)) and the trapping states density (\( N_t \)). Finally, at higher doping concentration the grains become partially depleted and hence the barriers are reduced allowing for a rapid increase in conduction, eventually reaching saturation. Fig. 3 shows the variation of doping density at which mobility is minimum (\( N^* \)) as a function of grain size (\( D_G \)). To examine its validity the experimental data are taken from Seto\(^{13}\). The decrease in \( N^* \) with increasing \( D_G \) may be attributed to the decrease in disorder of the material as it changes from poly- to single-crystal.

To validate the model the variation of effective carrier mobility/modeling factor (\( \mu_{eff}/f \)) versus doping
concentration taking \( f = 0.04 \) for \( n_g = 500 \) taking \( D_G = 20 \text{ nm} \) \( \text{(Seto)}^{13} \) is shown in Fig. 4 and is compared with the experimental values of Seto\(^{13} \). The computed variation was found to account correctly for the experimentally observed mobility variation and yield a reasonable good agreement.

Figs 5 and 6 show the computed variations of effective carrier mobility \( (\mu_{\text{eff}}) \) versus gate voltage \( (V_G) \) and drain current \( (I_D) \) versus gate voltage \( (V_G) \) for \( D_G = 50, 100, 300, 500 \) and \( 1000 \text{ nm} \) in the channel at room temperature.

It is found that at low gate voltages, the values of \( \mu_{\text{eff}} \) and \( I_D \) increase rapidly with the increase in \( V_G \) for all values of grain sizes. It may be due to the grain boundary barrier lowering effect. The decrease in grain boundary barrier height with increasing gate voltage is attributed to an increase in induced carrier density in the channel. At high gate voltage the grain boundary barrier lowering effect becomes insignificant and causes the saturation of \( \mu_{\text{eff}} \) and \( I_D \).

The barrier lowering is expected to be slower because the Fermi-level is being pulled more slowly towards the conduction band. The saturation of \( \mu_{\text{eff}} \) and \( I_D \) occurs because most of the applied gate voltage is...
used to charge these states and not to induce free carriers in the channel. It is also observed that as grain size increases the values of $\mu_{\text{eff}}$ and $I_D$ increase, which is mainly due to the reduction in number of GBs in the channel. To verify the model the experimental variations were taken from Kong et al.\textsuperscript{12} for $D_G = 100$ nm.

4 Conclusion

The grain size of poly-Si plays a dominant role in determining the potential barrier height at the grain boundaries, effective carrier mobility ($\mu_{\text{eff}}$) in the channel and transfer characteristic of poly-Si TFT. For the fixed number of grains of a fixed grain size in the channel, the mobility decreases with increasing doping concentration passes through a minimum and then increases. With the increase in the number of grains in the channel or decrease in the grain size of a poly-Si TFT, the poly-Si mobility and drain current decrease with gate voltage. In order to validate our model we compared the theoretically predicted results with the experimentally observed variations, and found a reasonably good agreement. The model thus gives theoretical understanding in its simple form, about the effect of grain size and doping concentration on the mobility of poly-Si TFTs.

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