On the jitter performance of a quantizer based modified DPLL

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The paper examines the effect of an additional derivative control signal (ADCS) on the steady state phase jitter characteristics of first and second order digital phase locked loops (DPLLs) having a finite level quantizer. It has been shown that the ADCS reduces the steady state phase jitter variance particularly when the DPLL gain parameters are high and the input signal has large frequency detuning. Further, a prefixed amount of SSPJ variance can be achieved in presence of the ADCS for a loop with a quantizer having lesser number of levels. The simulation results obtained have been qualitatively interpreted.

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Conventional digital phase locked loops (CDPLLs) are widely used in data receivers and modems as timing synchronizers, carrier synchronizers and frequency synthesizers1-3. In a practical CDPLL, a finite level quantizer is included to generate the control signal of the loop digitally controlled oscillator (DCO)4,5. It results in quantization of the DCO frequency; as such the steady state phase error shows a jittery fluctuation without converging to a fixed value. In recent years, the dynamics of the phase jitter process has been extensively studied through computer simulation6 as well as analytically7,8 by different authors. Since the quantization process is highly non-linear in nature, one cannot analyze the global behaviour of the dynamics of the system completely6. Nevertheless, the findings of these studies are useful in designing an optimum DPLL.

From the designer point of view, a quantizer based DPLL should have the following salient features:

First, quantizing phase jitter should be less as practicable as possible. Quantizing phase jitter is quantified by the following relation6

\[
\delta f = \frac{1}{2^b T} \text{ Hz}
\]  

where, \(1/T\) is the clock frequency of the DCO and \(b\) is the number of bits in the register, i.e., \(2^b\) represents the number of quantizer levels. Eq. (1) tells that, a finite length of the register introduces a quantizing phase jitter in the loop even in its steady state of operation. To reduce this jitter, \(b\) should be as large as practicable. But, a longer register length results in power consumption, high cost, low speed and larger chip area6. Therefore, there is always a motivation to modify the conventional DPLL (CDPLL) in a way, such that it produces lower phase jitter even with smaller register length (b).

Second, the DPLL should have larger acquisition range without degrading its transient characteristics. For a first order DPLL, acquisition range increases with the increasing loop gain parameter \(K_1\) up to its stability limit. So, to achieve larger acquisition range, a first order loop should operate with large loop gain. Also, a second order DPLL should have to withstand a larger signal detuning condition to show a large acquisition range. But, larger loop gain and detuning results in increasing quantizing phase jitter variance6. So, a smaller jitter variance and larger acquisition range cannot be achieved simultaneously. Therefore, this situation also demands a modification of CDPLL.

The present work describes a suitable modification of a CDPLL such that the quantizing phase jitter can be reduced even in its small register length, large loop gain and signal detuning condition. This modification was first used to improve the transient response of a quantizer less first order DPLL9. Here, a differentiator arm is introduced in a CDPLL along with the loop digital filter (LDF) (Fig. 1). The output of the differentiator arm is the additional derivative control signal (ADCS). The ultimate structure modification reduced to a PD (proportional plus differentiator) controller for a first order DPLL and a PID (proportional plus integrator plus differentiator) controller for a second order DPLL. As is common in PD and PID controller, the differentiator arm

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improves the gain margin and phase margin of the loop, so intuitively one can say that the modification may reduce the phase jitter. The system behaviour has been studied numerically through computer simulation. It is established that the modified DPLL has the ability in reducing the phase jitter variance compared to that of a CDPLL even with a smaller number of quantizer levels and at the same time larger loop gain and signal detuning. Efforts are taken to interpret some of the findings from the qualitative point of view.

**Structure and System Equation**

Figure 1a shows the functional block diagram of a general DPLL having the proposed modification of the structure. Figs 1b and 1c represent the structure of the loop digital filter (LDF) for first order and second order DPLL, respectively. To obtain the system equation of the loop, consider the input signal $s(t)$ as:

$$s(t) = A \sin(\omega_t t + \theta_0) \quad \ldots(2)$$

where $A$, $\omega_t$ and $\theta_0$ are the amplitude, angular frequency and phase of the input signal respectively. Consider that $\omega_0$ is the DCO nominal frequency (period $T$) and $\theta_0(t)$ as $(\omega_t - \omega_0)t + \theta_0$, then the sampler output at the $k$-th sampling instant $t(k)$ is

$$x_c(k) = A \sin(\omega_0 t(k) + \theta_0) \quad \ldots(3)$$

In the modified DPLL proposed earlier, the ADCS is generated as $x_c(k) = P[x_c(k) - x_c(k-1)]$, where $x_c(k-1)$ is the sampler output at the sampling instant $t(k-1)$ and $P$ is the difference amplifier gain. The total control signal at the $k$-th sampling instant is the sum of the conventional sampled value and ADCS given by $x(k) = x_c(k) + x_c(k-1)$, i.e.,

$$x(k) = (1 + P)x_c(k) - P x_c(k-1) \quad \ldots(4)$$

The sequence $\{x(k)\}, k = 0, 1, 2, \ldots$ is filtered digitally by a suitable loop digital filter (LDF) to get the LDF output sequence as $\{y(k)\}, k = 0, 1, 2, \ldots$. The quantized version of $\{y(k)\}$ is used to control the next period of the DCO. The algorithm of the quantizer is described by the relation,

$$Qnt[y] = \frac{1}{2^b} \text{Int}[v \cdot 2^b] \quad \ldots(5)$$

where $v$ is the variable to be quantized, $\text{Int}[]$ denotes the integer part of the argument and $b$ is the length of quantized word expressed using binary digits. It is obvious that $2^b$ stands for the total number of levels of the quantizer. Now, the next sampling instant $t(k+1)$ can be written as

$$t(k+1) = t(k) + T(k+1) \quad \ldots(6)$$

and DCO period $T(k+1)$ at that instant is governed by the relation

$$T(k+1) = T - y_q(k) \quad \ldots(7)$$

where $y_q(k) = Qnt[y(k)]$ is the quantized control signal of the DPLL at the $k$-th sampling instant. Assuming $t(0) = 0$, we get

$$t(k) = kT - \sum_{i=0}^{k-1} y_q(i) \quad \ldots(8)$$

thus the sampler output at the $k$-th instant is,
where
\[ \phi(k) = \theta_i(k) - \omega_\phi \sum_{i=0}^{k-1} y_i(i) \]  

is the phase error between the input signal and the DCO output at \( t(k) \). For a second order DPLL, the output of the LDF can be written as
\[ y(k) = (G_1 + G_2) x(k) + G_2 \sum_{i=0}^{k-1} x(i) \]  

Here \( G_1 \) and \( G_2 \) are the gains of the proportional and the delayed arms of the LDF, respectively. Now, one can write the difference equation governing the system behaviour of the second order modified DPLL in the face of noise free unmodulated input signal, as,
\[ \phi(k+1) = \phi(k) + 2\pi(z-1) - \omega_\phi z Q n t[y(k)]. \]  

Here, we have substituted \( z = \left[ \frac{\omega_\phi}{\omega_0} \right] \). By putting \( G_2 = 0 \), Eq. (12) reduces to the system equation of first order modified DPLL. Further with \( P = 0 \), Eq. (12) represents the system governing equation for CDPLL. It is evident from the system equation that, because of the presence of the quantizer a fixed steady state value of \( \phi(k) \) cannot be obtained in general for a given \( z \). The quantizer output will change in steps by an amount of \( 2^b \) units in each step and hence a steady state jitter will be observed in the magnitude of \( \phi(k) \).

**Results and Discussion**

An extensive simulation study has been carried out to examine the performance of the CDPLL and modified DPLL in the face of a noise free unmodulated frequency step input using the system equation (Eq. 12). The response of the loop has also been studied considering the ideal transfer functions of the hardware blocks of the DPLLs (Fig. 1). \( K_1 \) and \( K_2 \) are two system parameters used in the places of \( \omega_0 AG_1 \) and \( \omega_0 AG_2 \). This has been done to keep similarity of notations as used in DPLL literature; also for second order DPLL one takes \( r = 1 + (K_2/K_1) \) as an additional design parameter.

Different values of parameters \( K_1, K_2, r, b \) and \( P \) are used to understand their relative influence on the jitter performance of the CDPLL and the modified DPLL. Further, in all the simulations we consider the range of values of the parameters for which the loop remains in its stable mode of operation, i.e., we do not consider the out-of-lock conditions. Thus, for first order loop \( K_1 \) should obey the stability condition\(^2\) \( 0 < K_1 < 2 \) (for phase step input) and \( 0 < (K_1^2 z^2 - \Lambda_0^2) < 4 \) (for frequency step input) with \( \Lambda_0 = 2\pi(z-1) \). Also, for the second order loop \( K_1, z \) and \( r \) should be restricted to the condition\(^2\) \( 0 < K_1 z < \frac{4}{(1+r)} \).

**Effect of the loop gain parameters**

The effect of the loop gain parameters with different detuning ratio (\( z \)) has been explored for a particular value of quantizer level. Here, we choose \( b = 6 \), because a commercially available DCO commonly use this value. Figure 2a depicts the variation of quantizing phase jitter variance (\( \sigma^2_\phi \)) with \( K_1 \). It shows that \( \sigma^2_\phi \) remains almost unaltered up to \( K_1 = 1.5 \) and after that it increases rapidly with \( K_1 \). Fig. 2b shows the variation of steady state phase jitter

![Fig. 2a— Variation of phase error variance (\( \sigma^2_\phi \), rad²) of First order CDPLL with the loop gain \( K_1 \) for \( b = 6 \) and \( z = 1.1 \)](image)

![Fig. 2b— Variation of steady state phase jitter (\( \phi_{ss} \), rad) with loop gain \( K_1 \) for a first order CDPLL (\( z = 1.1, b = 6 \)).](image)
with different loop gain $K_1$. It also shows that the peak to peak excursion of the steady state phase jitter becomes broader with the increasing $K_1$ after $K_1 = 1.5$. Fig. 2c shows that $\sigma^2_\phi$ increases with $K_1$ for a second order CDPLL. Here, we take $r = 2$, since it is the optimum value of $r$. Variation of $\sigma^2_\phi$ with different $r$ (with $K_1 = 1$) are shown in Fig. 2d. It also demonstrates an increasing $\sigma^2_\phi$ with increasing $r$. The increase of phase jitter variance with loop gain parameters is due to increased amount of quantizer output at those conditions. Also, from Fig. 2b, it is seen that the first order quantizer based CDPLL goes to unlocked region much before than $K_1 = 2$, i.e. use of quantizer makes the stability range narrower. So, for a higher value of $K_1 (> 1.5)$ there is a tendency of the loop to lose the locked condition depending upon the signal conditions. This in turn increases the phase jitter variance of the loop for $K_1>1.5$. The same argument is also true for the second order CDPLL.

**Response of the first order modified DPLL**

For a first order modified loop the variation of $\sigma^2_\phi$ with the parameter $P$ for different values of $K_1$ has been shown in Fig. 3a, when $z = 1.1$ and $b = 6$. It is evident that an optimum value of $P$ can be chosen which minimizes the value of $\sigma^2_\phi$ compared to the same when $P = 0$. Figure 3b shows the variation of optimum $P$ with $K_1$ which should be taken to obtain minimum $\sigma^2_\phi$. It is evident that, a proper choice of $P$
in a modified DPLL will be able to reduce $\sigma^2_\phi$ even with lower values of $b$. Further, the variation of peak to peak phase jitter as a function of $K_i$ has been shown for a modified first order DPLL (Fig. 3c), with $P = -0.1$. We choose this value of $P$ because Fig. 3a shows that the optimum value of $P$ is approximately around $P = -0.1$. It shows that the peak to peak excursion of the steady state phase error is less even with larger $K_i$ values. Comparing it with Fig. 2b ($P = 0$), it can be noticed that a proper value of $P$ can reduce the quantizing phase jitter even with a larger value of loop gain ($K_i$), which is our desired requirement. This observation can be interpreted in the following manner: the stability condition of a first order modified DPLL is shown to be\(^\text{10}\)

$$0 < K_i(1 + 2P) < 2 . \text{ For phase step input (}z = 1\text{)} \quad \ldots(13a)$$

$$0 < (K_i^2z^2 - \Lambda_b^2)(1 + 2P)^2 < 4 \text{ For frequency step input (}z \neq 1\text{)} \quad \ldots(13b)$$

It is evident from (13), that the effective gain value of modified DPLL depends on the $P$. negative value of $P$ reduces the effective gain of the system which in turn reduces the jitter variance.

Response of the second order modified DPLL

The effect of structure modification in the case of a second order CDPLL is evident from the simulation results. Taking the optimum values of $K_i$ and $r$ (i.e. $K_i=1$, $r=2$) the values of $\sigma^2_\phi$ is obtained for different values of signal detuning (different $z$) with $P = 0$ (CDPLL). Then, an optimum value of $P$ is obtained for each value of $z$ which minimizes $\sigma^2_\phi$ in the case of a modified DPLL. The results obtained indicate that the modified DPLL is capable of reducing phase jitter variance even with the larger signal detuning. The result of simulation study in this case is shown in Fig. 4. These results are also consistent with our prediction. The observations can be interpreted as the consequence of reduction in the effective gain parameters as before. The stability condition of second order MDPLL is given by\(^\text{10}\)

$$0 < K_i(1 + 2P) < \frac{4}{(1 + r)} \quad \ldots(14)$$

A negative $P$ value reduces the effective gain parameter and thus the steady state phase jitter variance reduces to some extent.
Jitter reduction of modified DPLL

Simulation studies have been carried out for the sake of comparison of $\sigma_\phi^2$ of CDPLL and modified DPLL with different values of $b$. Figure 5a shows that for a first order DPLL and Fig. 5b shows the same for the second order DPLL. It is obvious from the two plots that modified DPLL has an ability to reduce the phase jitter without increasing the value of $b$. An interesting result has been revealed from the simulation that, the modified DPLL shows lower $\sigma_\phi^2$ even with a smaller value of $b$ for a higher signal detuning. Figure 5c shows this for a second order DPLL and it can be seen that CDPLL with $b = 7$ shows higher $\sigma_\phi^2$ than that of the modified DPLL with $b = 6$ in the higher signal detuning ($z$). It is important from the viewpoint of DPLL hardware designer in the sense that one can now design a DPLL with reduced phase jitter even with smaller $b$.

Time domain representation of phase jitter

The variation of steady state phase error at consecutive sampling instants is shown in Figs 6a and 6b for a first order CDPLL and first order modified DPLL, respectively, with optimum $P$. Figures 7a and 7b show the same results for a second order case. The range of peak-to-peak variation of the phase error is lower for a modified DPLL which again substantiates the better performance of the modified loop.

The present work shows that the modified DPLL has got improved phase jitter performance compared to a CDPLL even in the presence of a finite level quantizer in the loop. Through a detailed simulation study on the performance of the conventional and modified DPLLs it has been shown that a proper choice of the structure parameter ($P$) of the modified loop, the variance of the phase jitter can be minimized. However, the choice of $P$ is more critical in the case of second order system as it depends on the signal detuning also. Qualitatively the improved response of the modified loop can be explained in the following way: since the additional error signal used in the modified loop is proportional to the instantaneous phase error of the loop, the loop has an ability to compensate the fluctuation of the quantized phase errors relatively quickly. The peak-to-peak fluctuation of the phase error would be less in the case of the modified loop. However, the fluctuation of the phase error cannot be made zero because this fluctuation is an inherent problem of a quantizer based DPLL. The design algorithm of the quantizer indicates that when all other parameters of the loop remain same, the step size of the quantizer increases...
with the increase of the loop gain parameters. The
effect of the ADCS used in the modified loop is to
reduce the loop gain parameters and hence the jitter
response of the modified loop is better than that of the
conventional loop.

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