Variation of width of the hysteresis loop with temperature in an emitter-coupled Schmitt trigger

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Schmitt trigger circuits are designed with pnp transistors: the first circuit with two 2SB324 germanium transistors, and the second one with two U188 silicon transistors. At certain collector resistances in the second stage— or the driven— transistor, the variations of the hysteresis loop width in temperature range –95-75°C for the first circuit, and 100-150°C for the second one have been observed. The increase in the loop width with temperature is shown.

Keywords: Hysteresis loop, Schmitt trigger, Transistor cut-off, Transistor saturation
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1 Introduction

The Schmitt trigger is a special class of gate, which is characterized by improved noise immunity and wave-shaping capability. This simple electronic bistable system converts a slowly varying input voltage into an output waveform displaying an abrupt, almost discontinuous change that occurs at a precise value of the input voltage. The Schmitt trigger can be understood in the framework of a two-well potential—a feature that has been made use of in the study of the stochastic resonance in the presence of an external periodic forcing. This regenerative comparator can be made of discrete components like TTL, and also specially designed ICs like CMOS Schmitt trigger, Quad 2-input NAND Schmitt trigger, Hex Schmitt trigger. Recently, an emitter-coupled Schmitt trigger, with both transistors of the type 2n2222, has been driven with a high-frequency signal to look for non-linear effects that disrupt the operation of circuits. In a circuit to detect a soft error in an SRAM cell, Schmitt triggers have been employed. In the Quad 2-input NAND Schmitt trigger, the hysteresis loop is determined by resistor ratios and is insensitive to temperature and supply variations, while the same in Hex and CMOS Schmitt trigger shows a low variation with temperature of the order of 0.0005 V/°C. Studies on the dependence of the hysteresis loop on other factors are presented in a number of papers. There have been a few relevant reports about the thermal effects on transistor parameters, such as doubling of reverse saturation current $I_{CO}$ for every 10°C increase in temperature, variations of $h_{FE}$ and $h_{RE}$ with temperature, decrease of 2 mV base-emitter voltage at a certain base current per degree centigrade increase of junction temperature. Switching hysteresis range, changed by substituting passive components such as resistors, has been used in the design of a constant current, fast and float rate, variable hysteresis battery charger. A survey of literature indicates that the thermal effect on the loop width of an emitter-coupled Schmitt trigger has not been studied so far. In this work, variation of the hysteresis loop width of emitter-coupled germanium and silicon transistor-based Schmitt triggers at different temperatures is shown.

2 Experimental Details

The circuit diagram of the Schmitt trigger is shown in Fig. 1. —Circuit diagram of the emitter-coupled Schmitt trigger. $R_{1}$=2.9 kΩ, $R_{2}$=3.9 kΩ, $C$ = 0.1 μF, $R_{3}$=3.9 kΩ, $R_{4}$=5.8 kΩ, $R_{5}$=670 Ω. In the circuit with transistors 2SB324 (Q1 and Q2), $R_{6}$=1 kΩ, and in the circuit with transistors U188, $R_{7}$=820 Ω.
in Fig. 1. The collector supply and various input voltages are obtained from OMEGA IC regulated power supplies. Since an extremely stable collector supply voltage is imperative for a work of this kind, the input to the regulated power supply is taken from an APC Back-UPS ES 500. The two transistors and the probe of a JULABO thermometer are kept in a test tube. For recordings at high temperatures, the test tube is placed inside a VEB MLW PRUFGERATWERK circulation thermostat whereby the required temperatures are obtained. Readings of the input and output voltages are noted from MASTECH multimeters. For low temperature recordings, a specially designed container, made from thick thermocore, is used to keep a few litres of liquid nitrogen at the bottom and the test tube is gradually inserted inside the container, whereby the required ambient temperatures are obtained. It is ensured that emitters, bases and collectors are not shorted, and also that the temperature changes encountered by the transistors are gradual. In this arrangement, two 2SB324 transistors with approximately equal β (~190) are used at first. Then, the two germanium transistors are replaced by U188 silicon transistors (β~220).

3 Results and Discussion

Initially, the first stage transistor Q1 has no forward bias and is cut-off. So, the emitter-base junction of the second stage transistor Q2 is forward biased, and it is turned on. The output gives us the lower voltage level of the trigger. Because of the saturation current in Q2, there would be a voltage drop across the 3.9 kΩ emitter resistor—which is common to both the transistors—adding to the potential barrier of the emitter-base junction of Q1. As soon as the input voltage exceeds this total reverse voltage, Q1 would conduct. This turns off Q2 and hence we get the upper voltage level of the trigger. By gradually reducing the input voltage, Q1 is cut-off at a voltage which is lower than the one at which the upper triggering took place. The difference between the upper trip point (UTP) and the lower trip point (LTP) gives the hysteresis voltage. At a high temperature, such as 75°C for the circuit designed with germanium transistors, because $h_{FE}$ would be high $^{10,11}$, greater emitter current in Q2 makes the voltage drop across the emitter resistor higher which makes the upper trip point higher. Consequent lowering of the temperature, up to −95°C in the same work, would make the emitter-base reverse bias of Q1 low, thus requiring a lower voltage for the upper trigger. The change in the LTP is minimal, probably due to the fact that changes in $V_{BE}$ and β with temperature are approximately proportional; the slight decrease of this point could mean that the decrease of β at lower temperature is proportionately more than the increase of $V_{BE}$. For the Q2 collector resistance of 1 kΩ, the hysteresis loop width at temperatures −95, −20, −35 and −75°C are given in Table 1, and the outputs from the transistor Q2 at the maximum (75°C) and minimum temperatures (−95°C) are shown in Fig. 2. An interesting observation with the circuit designed with silicon transistors is that the UTP changes little compared to the LTP. For the Q2 collector resistance

<table>
<thead>
<tr>
<th>Temperature °C</th>
<th>Upper trip point V</th>
<th>Lower trip point V</th>
<th>Loop width V</th>
</tr>
</thead>
<tbody>
<tr>
<td>−95</td>
<td>5.29</td>
<td>4.05</td>
<td>1.24</td>
</tr>
<tr>
<td>−20</td>
<td>5.39</td>
<td>4.04</td>
<td>1.35</td>
</tr>
<tr>
<td>−35</td>
<td>5.42</td>
<td>3.99</td>
<td>1.43</td>
</tr>
<tr>
<td>−75</td>
<td>5.46</td>
<td>3.99</td>
<td>1.47</td>
</tr>
</tbody>
</table>

Table 1—Width of the hysteresis loop at different temperatures for the emitter-coupled Schmitt trigger designed with 2SB324 germanium transistors

![Fig. 2](image-url)
of 820 Ω, the hysteresis loop width at temperatures 100, 85, 65, 35, 20 and 150°C are given in Table 2. Very small change in the loop width from 20 to 150°C is definitely a pointer to the fact that changes in β are small in this range. On the other hand, relatively larger changes in LTPs at small temperatures could be due to the increase of $V_{BE}$, as changes in β with temperature in silicon transistors are relatively smaller than germanium transistors. The outputs from the transistor Q2 in this case for the two extreme temperatures are shown in Fig. 3. The changes in the width of the hysteresis loop for the two transistors are plotted in Fig. 4.

### Table 2—Width of the hysteresis loop at different temperatures for the emitter-coupled Schmitt trigger designed with U188 silicon transistors

<table>
<thead>
<tr>
<th>Temperature °C</th>
<th>Upper trip point V</th>
<th>Lower trip point V</th>
<th>Loop width V</th>
</tr>
</thead>
<tbody>
<tr>
<td>−100</td>
<td>5.34</td>
<td>4.28</td>
<td>1.05</td>
</tr>
<tr>
<td>−85</td>
<td>5.35</td>
<td>4.25</td>
<td>1.10</td>
</tr>
<tr>
<td>−65</td>
<td>5.38</td>
<td>4.24</td>
<td>1.14</td>
</tr>
<tr>
<td>−35</td>
<td>5.38</td>
<td>4.19</td>
<td>1.19</td>
</tr>
<tr>
<td>+20</td>
<td>5.38</td>
<td>4.14</td>
<td>1.24</td>
</tr>
<tr>
<td>+150</td>
<td>5.39</td>
<td>4.14</td>
<td>1.25</td>
</tr>
</tbody>
</table>

4 Conclusion

As is evident from Table 1, there is a change in the loop width of 110 mV for a change in temperature from −95 to −20°C (total change of −75°C), a change of 80 mV for a change from −20 to 35°C (total change of 55°C), and a change of 40 mV for a change from 35 to 75°C (total change of 40°C). The pattern of change in the second circuit is approximately same, but the changes, perhaps expectedly, are by lesser amounts. There is a change of 50 mV from 100 to 85°C, a change of 40 mV from 85 to 65°C, a change of 50 mV from 65 to 35°C, a change of 50 mV from 35 to 20°C, and a change of only 10 mV from 20 to 150°C. It is worthwhile to mention here that the variation has been found to be lower for higher collector resistances in the second stage transistor. This work qualitatively verifies earlier reports on the variation of transistor parameters $h_{FE}$ or $h_{ie}$ and $V_{BE}$ with temperature.

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