Analytical modelling of carrier transport through transverse and longitudinal grain boundaries in polysilicon thin-film transistors

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Carrier transport through transverse and longitudinal grain boundaries (GBs) in polysilicon thin film transistors (poly-Si TFTs) has been studied. The model considers an array of square grains in the channel of poly-Si TFT in which current flows along the longitudinal GBs and through the grains and the transverse GBs. The variation of field-effect mobility (μFE) and drain current (ID) is computed for different values of grain size. This study reveals that at low gate voltage the longitudinal GBs are seen to influence the field-effect mobility and drain current. As gate voltage increases, the effect of transverse GBs is found to account for experimental results. This is attributed to the fact that at low gate voltage, the carriers moving through longitudinal GBs have more opportunities to be trapped at the trapping sites and as gate voltage increases the carriers have sufficient energy to bypass the longitudinal GBs and obstructed by transverse GBs alone. This may be the reason that the calculated effects of longitudinal GBs do not appear in the experimental results at high gate voltage.

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Polysilicon thin-film transistors (poly-Si TFTs) with desirable electrical characteristics have been used for integrating driver circuits and pixel transistors on the same glass panel for active matrix liquid crystal displays (LCDs) and system-on-panel applications1,2. In poly-Si TFTs, carrier transport occurs in poly-Si films that include grains and grain boundaries (GBs). Grain boundaries, although physically much smaller than the individual grains, greatly influence the conduction properties of the material. GB defects not only trap and reduce free carriers, but also forms potential barriers and interfere with carrier movement. Perpendicular GBs was considered in the reports that have analyzed the carrier transport over GBs in poly-Si films and poly-Si TFTs3-14; carrier transport along GBs was hardly considered15 and no analytical model was developed as such.

In the present model, it is assumed that the longitudinal GBs is along the full length of the device and current transport, from source to drain, takes place in two ways: along GBs (longitudinal) and through the grains and across GBs (transverse). The width of these grain boundary regions is arbitrary fixed for the purpose of this calculation. The mobilities are assumed to be different in each of these different areas of the grain in the channel. It is also assumed that the carrier distribution is uniform throughout the channel of the device and all induced carriers contribute to the conduction once the gate voltage is beyond the threshold voltage. But this assumption is not true if the GBs act as trap carriers and form depletion regions.

Therefore, the aim of this paper is to analyze the transistor characteristics due to the carrier transport through transverse and longitudinal GBs in poly-Si TFTs by developing an analytical model.

Theory

Fig. 1a shows the schematic diagram of the channel of polysilicon TFT showing the current passing through grains and passing across and along GBs and Fig. 1b shows the cross-sectional view of poly-Si TFT. Let n be the number of grains in the channel and D_G be the average grain size within a TFT. The length of the device can be expressed as

\[ D_{\text{eff}} = n \cdot D_G = n \cdot (D_{\text{Gi}} + D_{\text{GB}}) \]  

where \( D_{\text{GB}} \) is the grain boundary width.

Assuming that the carrier conduction is uniform throughout the active layer and all induced carriers contribute to the conduction once the gate voltage is beyond the threshold voltage, the drain current can be expressed as\(^{16}\):

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where \( \mu_{FE} \) is the field-effect mobility, \( C_{ox} (= \varepsilon_{ox}/t_{ox} \) where \( \varepsilon_{ox} \) is the dielectric permittivity of oxide film and \( t_{ox} \) is the thickness of oxide film) is gate oxide capacitance per unit area, \( V_T \) is threshold voltage, \( V_G \) is gate voltage and \( V_D \) is drain voltage of a poly-Si TFT. Writing Eq. (2) as:

\[
I_D = \frac{\mu_{FE} Z_{Cox}}{D_{eff}} [(V_G - V_T)V_D] \quad \ldots (2)
\]

The middle bracketed term in Eq. (3) is the assumed carrier density \( Q_c \). Hence

\[
Q_c = C_{ox} (V_G - V_T) \quad \ldots (4)
\]

The current flowing along the grain boundaries can be expressed as

\[
I_{D(||)} = Z_{(||)} Q_c (\mu_{GB(||)} V_D/D_{eff}) \quad \ldots (5)
\]

where \( \mu_{GB(||)} \) is the mobility for a carrier passing along a GB and \( Z_{(||)} \) is the total width of these GB regions. To calculate the current passing through the middle of the grains is not easy, first it is expressed as:

\[
I_{D(G)} = Z_{(G)} Q_c (\mu_G V_D/D_{eff}) \quad \ldots (6)
\]

where \( \mu_G \) is the net mobility for the current passing through the grain interiors and across GBs and \( Z_{(G)} \) is the length of these regions. Now making use of current continuity, the current can also be calculated inside the grain and across the grain boundary.

Taking contribution of grain interior mobility \( \mu_G \) and transverse boundary mobility \( \mu_{GB(\perp)} \) we can express \( \mu_G \) empirically as

\[
1/\mu_G = 1/(\mu_G + 1/\mu_{GB(\perp)}) = 1/(\mu_G + 1/\mu_o \exp(-q\psi_B/kT)) \quad \ldots (7)
\]

where \( \mu_o \) is the prefactor of \( \mu_{GB(\perp)} \) and \( \psi_B \) is the potential barrier height. \( \mu_G \) has higher values, as the grain interiors, while defective, are close to single crystals, \( \mu_{GB(\perp)} \) incorporates both scattering when the carriers penetrate the GBs and the reduced carrier density near the GBs when compared to the grain interiors. Hence \( \mu_G /\mu_{GB(\perp)} \).

Now Eq. (7) becomes

\[
\mu_G \approx \mu_o \exp(-q\psi_B/kT) \quad \ldots (8)
\]

The total current is the sum of the current along the GBs, \( I_{D(||)} \) and through the middle of the grains, \( I_{D(G)} \)

\[
I_{D}=I_{D(||)}+I_{D(G)} \quad \ldots (9)
\]

From Eqs (3), (5) and (6) we have

\[
\mu_{FE} = (Z_{(||)}/Z) \cdot (Z_{(G)}/Z) \cdot \mu_G \quad \ldots (10)
\]

Using Eq. (1) above equation can also be written as

\[
\mu_{FE} = (D_{GB}/D_G) \cdot \mu_{GB(||)} + (D_G/D_G) \cdot \mu_G \quad \ldots (11)
\]

Putting the values of \( \mu_G \) from Eq. (8), field-effect mobility can be written as:

\[
\mu_{FE} = (D_{GB}/D_G) \cdot \mu_{GB(||)} + (D_G/D_G) \cdot \mu_o \exp(-q\psi_B/kT)
\]

The values of potential barrier height (\( \psi_B \)) for a poly-Si TFT at room temperature, assuming monoenergetic traps at the grain boundaries, in the term of gate voltage is given by

\[
\psi_B = q^2 N_T^2 \varepsilon_s/8 \varepsilon_o C_{ox} (V_G - V_T) \quad \ldots (12)
\]

where \( \varepsilon_s \) is the polysilicon inversion layer thickness, \( N_T \) is the trap state density and \( \varepsilon_o \) is the dielectric permittivity of polysilicon. The trapping state density \( (N_T) \) is found to decrease with increasing grain size \( (D_G)^{1.8} \) which may be attributed to a decrease in disorder in larger grains. To incorporate this effect, an empirical relation between \( N_T \) and \( D_G \) which fits with the experimentally available value is given by:

\[
N_T = (35 + 2.55 D_G^{0.365}) \times 10^{10} \text{ cm}^{-2} \quad \ldots (13)
\]

For calculation the mobility values are taken from Wang et al.\(^{20} \) and Serikawa et al.\(^{17} \); \( \mu_{GB(||)} = 3 \text{ cm}^2\text{V}^{-1}\text{s}^{-1} \)

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Fig. 1 — (a) Schematic diagram of the channel of polysilicon TFT showing the current passing through grains and passing across and along GBs, and (b) cross-sectional view of poly-Si TFT.
and $\mu_0 = 11 \text{ cm}^2\text{V}^{-1}\text{s}^{-1}$. The other parameter taken are shown in Table 1.

**Results and Discussion**

Carrier transport through longitudinal and transverse grain boundaries in poly-Si TFT has been studied. Field-effect mobility ($\mu_{FE}$) and drain current ($I_D$) are computed for small drain voltage ($V_D = 0.1 \text{ V}$) at room temperature for different grain sizes as a function of gate voltage ($V_G$). Figs 2a and 3 shows the computed variations of $\mu_{FE}$ and $I_D$ with gate voltage for grain size ranging from 50 nm to 2500 nm. It is observed that at low gate voltages, $\mu_{FE}$ and $I_D$ increases with gate bias due to the gate-induced free carrier concentration. At high gate voltages, $\mu_{FE}$ reaches to more or less a saturation value. Possible reasons for the saturation are a scattering of carriers due to an increase in the vertical electric field strength in the channel and parasitic resistance due to doped source and drain regions. Fig. 4 shows the effect of longitudinal GBs on the drain current as a function of gate voltage for $D_G = 100 \text{ nm}$. It is observed that at high gate voltage, longitudinal GBs have almost no effect on the drain current while at low gate voltage ($V_G < 5 \text{ V}$) there is little effect on the drain current, however, the experimental values\textsuperscript{18} matches with the computed variation of the drain current which is calculated without considering the contribution of longitudinal GBs. This is attributed to the fact that at low gate voltage, the carriers moving through longitudinal GBs have more opportunities to be trapped at the trapping sites and as gate voltage increases the carriers have sufficient energy to bypass the longitudinal GBs and obstructed by transverse GBs alone. This may be the reason that the calculated effects of longitudinal GBs do not appear in the experimental results at high gate voltage.

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<thead>
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<th>Table 1— Parameters for calculating poly-Si mobility and drain current as a function of gate voltage</th>
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<td>Parameters</td>
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<td>Oxide film thickness</td>
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<td>Gate oxide capacitance per unit area</td>
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$\mu_{FE}$ is the field-effect mobility, $I_D$ is the drain current, $V_D$ is the drain voltage, $V_G$ is the gate voltage, $D_G$ is the grain size, $t_{si}$ is the polysilicon inversion layer thickness, $t_{OX}$ is the oxide film thickness, $C_{ox}$ is the gate oxide capacitance per unit area.
The trend of the model for $\mu_{FE} - V_G$ plot shown in Fig. 2a is same as the experimentally observed variations; however for the best fit of exact values, a modelling factor $f$ is introduced in the field-effect mobility. To validate the model, the computed variations of $\mu_{FE}/f$ as a function of $V_G$ taking $f = 0.465$ for $D_G = 500$ nm shown in Fig. 2b is compared with the experimental values of Seki et al. The computed variations are in excellent agreement with experimental results confirming the validity of the model.

Conclusions
In this paper, an analytical mobility model considering the effect of transverse and longitudinal GBs on $I$-$V$ characteristics of poly-Si TFTs has been presented. This study reveals that at low gate voltage the longitudinal GBs influence the field-effect mobility and drain current. As gate voltage increases the effect of longitudinal GBs have no effect on the characteristics of poly-Si TFT. The experimental results agree fairly well with the $I$-$V$ characteristics obtained by neglecting the effect of longitudinal GBs and considering only the transverse GBs.

References