Indian Journal of Engineering & Materials Sciences
Vol. 13, February 2006, pp. 55-61

Investigation of a power FLIMOSFET based on two-dimensional numerical simulations

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Received 28 February 2005; accepted 13 October 2005

This paper presents the numerical simulation results for a power FLIMOSFET structure with up to eleven vertical floating islands, designed using PISCES-IIB, a 2-dimensional advanced device simulator. The novel structure is based on the FLI-diode concept, which helps in lowering the maximum electrical field in the N^-epitaxial region of the device to reduce the effective on–resistance without degrading device performance. Extensive simulations were performed to understand the device physics through various internal electrical quantities like potential distribution and electric field in different regions of the device both in on/off states. The effect of drift region doping on the device performance has been discussed. It is shown that the decrease in the drift region doping tends to decrease the electric field distribution and intermediate potential in this region thereby making its on-resistance lower than the value given by the conventional silicon limit. The device structure does not require any precise control of the boron implantation dose in the P^+ floating islands for charge balance as essential in case of super junction (SJ)/COOLMOS^{TM} devices. The process flow mechanism required to fabricate FLIMOSFET structure using multi-epitaxial technology has been discussed, which is less complex and less expansive than the super junction (SJ) devices technology.

IPC Code: H02M

Vertical double-diffused MOSFET (VDMOSFET) is the key component in switching mode power supply circuits and inverter systems. It is a very important device in many power electronic applications for its well-known intrinsic advantages such as high input impedance, short switching time and thermal stability. MOSFETs for power applications cannot be fabricated by merely scaling up low-power MOSFETs to the desired voltage and current. The high voltage blocking ability requires a large depletion area across the reverse-biased P-N^- (body/drift) junction of the VDMOSFET. Thus, the power VDMOSFET structure contains a low-doped epitaxial layer in series with the drain region to increase the drain-source breakdown voltage. Furthermore, it increases the current densities by providing vertical current flow lines[1,2].

An ideal power device should support high voltage in the off state and when turned 'on' should have a very small voltage drop and support a high current density. This means that the on resistance (R_{on}) should be very low. These low on-resistance MOSFETs are desired for reduction of power loss in a power system. But these are contradictory requirements according to the well known silicon limit [$R_{on} \propto B_v^{2.5}$][1,2] which addresses the trade-off between breakdown voltage (B_v) and $R_{on.}$ Thus, it is clear that R_{on} increases dramatically when a large B_v is required. This is the main limitation of VDMOSFET technology, which is otherwise superior due to its high speed. Because of this limitation, high-voltage applications have invariably employed devices such as IGBT (insulated gate bipolar transistor) and thyristors despite their lower speed.

Many power MOSFET configurations have been studied to reduce the on-resistance and addresses the trade-off between B_v and R_{on} such as trench power MOSFET[3-6], super junction devices (SJ)[7,8], COOLMOS^{TM} transistors[9-11], and reduction in the R_{on} has been studied so far in terms of optimum doping density, thickness and doping profile of the drift region, however, SJ MOSFET/COOLMOS^{TM} has made it possible to attain higher speeds and larger breakdown voltages simultaneously. In these devices[7-11] the drift layer is replaced by a super junction composed of P and N "pillars" which share vertical boundaries. This modification causes a noticeable change in the electric field profile within the device, thereby resulting in large breakdown voltage. The SJ devices are based on the charge compensation concept, which practically has the following difficulties: (i) the charge must be strictly controlled in the pillars; otherwise the breakdown

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voltage (B_v) decreases rapidly, (ii) deep doping into bulk to make pillars is required to minimize the number of iteration processes, (iii) as the total imbalanced charge increases with pillar depth, the realization of high voltage devices becomes increasingly difficult, (iv) also it is very difficult to make deep implantation due to crystalline damage caused by high energy implants, and (v) for voltage rating less than 180 V, the narrow SJ columns of width 4 μm or less are very difficult to fabricate and good charge balance between P and N columns cannot be maintained even if possible to fabricate. Until now, no SJ power MOSFET device has ever been made for voltage rating below 100 V (Ref. 12).

Recently, it has been proposed that these issues can be addressed in a novel structure having vertical floating islands introduced in the N^- epitaxial region of the conventional VDMOSFET known as FLIMOSFET[13-19]. These new vertical MOSFET structures are based on the "FLI-diode" concept, which states that the triangular electric field distribution in the bulk is divided into several sections to decrease the magnitude of the peak electric field by inserting electrically vertical floating P^+ buried layers in the N^- drift region as indicated in Fig. 1. The on-resistance reduction mechanism can be explained in the following manner. In the conventional VDMOSFET as shown in Fig.1a, the N^- drift region is required to be lightly doped so that the depletion region sufficiently develops into this area to sustain higher blocking voltage. The lightly doped N^- drift region results in higher value of the resistivity. Whereas in FLIMOSFET structure (Fig.1b), the P^+ floating layer increases the development of depletion layer due to a mechanism similar to the P-guard rings in planar terminations, i.e., once the source side reaches the P^+ floating layer, the voltage of this layer is lowered due to the punch-through between the P^+ floating layer and the P-base region, then a new depletion layer develops from the bottom of the P^+ floating layer towards the drain. With this mechanism, the doping concentration of the N^- epitaxial drift region can be enhanced which strongly reduces access (R_a) and drift (R_d) resistances, thereby reducing overall specific on-resistance by a factor equivalent to the enhancement in doping concentration. In FLIMOSFET, the drift region is divided into two sections, named upper and lower drift regions, by the insertion of the floating island. As the reverse bias is increased, the space charge region extends from the P-base region towards the floating island in the upper drift region. When this upper drift region is entirely depleted, then the space charge starts to extend from the bottom of the floating island towards the drain of the FLIMOSFET in the lower drift region. Thus, two electric field distributions, each of triangular shape are formed at both upper and lower drift regions, as shown in Fig. 1c. In contrast, a single electric field distribution is formed in case of conventional power VDMOSFET structure, also shown in Fig. 1c. Therefore, a number of consecutive vertical floating islands can be used to satisfy the desired device performance with designing the peak electric field in the FLIMOSFET kept below the critical electric field.

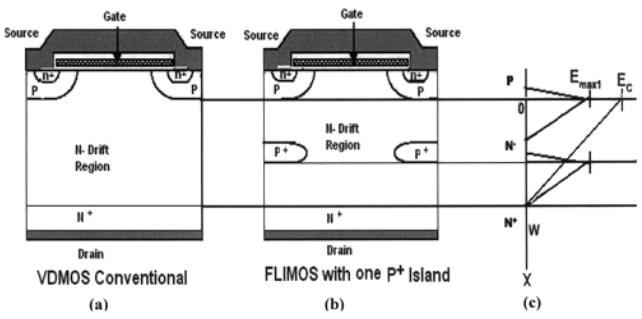

Fig. 1—FLI-diode concept: (a) a conventional VDMOSFET structure, (b) FLIMOST with the induction of one floating island (c) electric field reduction mechanism

The FLIMOSFET structure has a distinct advantage over the SJ structure on boron implantation dose control for the P^+ buried floating layer. The SJ structure is designed with the RESURF (reduced surface field) concept, where the implantation dose is to be severely controlled to compensate the space charge in the N^- drift region, which is not the case in FLIMOSFET. It has been shown that conventional VDMOSFET 'silicon limit' can be overcome by using FLIMOSFET structure, which appears to be one of the best power MOSFETs in low voltage applications.

Device Operation and Simulations

A power FLIMOSFET structure as shown in Fig. 2 is similar to a conventional VDMOSFET in the following aspects: (i) this structure is also based on the double diffusion of the P-body and N^+ source regions using the edge of the polysilicon as a masking boundary; (ii) there is a long vertical, low-doped drift region which enables the device to block high voltage; (iii) the gate overlaps both the channel and the drift region so that an accumulation layer is formed in the linear operating region to enhance the conductivity; (iv) the source contact overlaps the P-body region to short-circuit the source/body junction, ensuring that the parasitic BJT is normally

off; (v) the channel region has graded doping, and (vi) the drain contact is kept at bottom of the device, giving rise to vertical current flowlines. The FLIMOSFET structure differs from VDMOSFET only in its N^- epitaxial drift region design. In this paper, up to eleven P^+ vertical buried floating islands have been introduced in the N^- epitaxial drift region to study the impact of these islands on the device performance. With no bias on the gate terminal, the N^+ source and N^+ drain are separated by P-base region and no current flows (transistor is turned-off). If a positive bias is applied to the gate, the minority carriers in the P-base (electrons) are attracted to the surface underneath the gate electrode. As the bias increases, more electrons are being confined to this small space, the local "minority" concentration becomes larger than the hole (*p*) concentration and "inversion" occurs (meaning that the material immediately under the gate turns from *p*- to *n*-type). Now, an *n* "channel" is formed in the *p* material right under the gate structure connecting the source to the drain; current can now flow. Like in the case of the JFET (although the physical phenomenon is different), the gate (by means of its voltage bias) controls the flow of current between the source and the drain.

P^+ buried floating islands are incorporated in a part of the whole conduction surface of the device, allowing the circulation of the drain current in the other part of the device. The length of these P^+ islands is chosen in accordance with reported method[13]. In the off-state the device acts like a diode but the voltage handling capability of this structure is obtained by

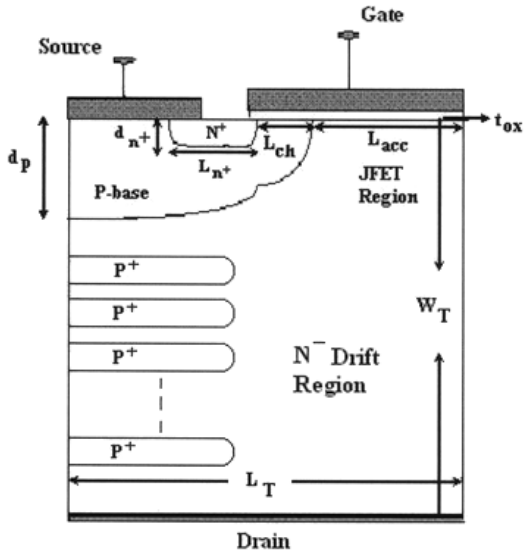

Fig. 2 — Schematic design of a FLIMOSFET transistor.

many P^+-N junctions in series whereas in the conventional VDMOSFET structure the breakdown voltage is supported by only one P-N junction. These floating islands reduce the maximum electric field at the junctions for the same doping and can assume an intermediate potential on either side of the junction which helps in lowering the specific on-resistance of the device as a result of the increase in the N^- drift region doping. The device simulations using PISCES-IIB[20] take into account the mobility model that is dependent on electric field, impurity concentration and impact ionization at a temperature of 300 K. In order to simplify the analysis, two-dimensional numerical simulation was carried out for only half of the unit cell since the device structure is symmetric as reported in the literature[15-17,21-23]. The geometrical dimensions along with the doping densities used for the device simulations are chosen to design a typical power FLIMOSFET in accordance with the various standard values used in similar devices [15-17,21-26] as given in Table 1.

The device structure is mapped onto a mesh, which can be refined to follow closely the contours of the device. The various regions of the device are then defined, doping profiles and concentrations specified, and electrodes placed at the appropriate positions. PISCES-IIB can solve for a variety of electrical quantities like potential, electric field, carrier and charge concentrations and currents under steady or transient bias conditions at the electrodes. The solution method used is Newton and both carrier types are considered. The effect of various physical mechanisms was included through 'model' statement. All the post-processing and graphical outputs are generated by POSTMINI[27] graphical post-processor.

Table 1— Design parameters used for FLIMOSFET simulation

Parameter	Value
L_{acc}	2.3 μm
L_{ch}	1.0 μm
L_T	4.0 μm
W_T	25.0 μm
t_{ox}	0.08 μm
d_p	1.5 μm
L_{n+}	0.5 μm
d_{n+}	0.2 μm
N_{n-}	5.0×10^{15} cm^{-3}
N_{n+}	5.0×10^{19} cm^{-3}
N_p	1.0×10^{17} cm^{-3}

Proposed Process Flow Mechanism

The technology to fabricate FLIMOSFET is still under active research and progress[14]. Here, we present a possible process flow sequence to fabricate FLIMOSFET commercially using multi-epitaxial layers. The process starts with a 0.002 to 0.004 Ω-cm, arsenic-doped <100> silicon substrate on top of which phosphorous-doped silicon drift region is to be epitaxially grown. The starting epitaxial region doping density N_{n-} can be kept within 1.0×10^{15} to 5.0×10^{15} cm^{-3} with a thickness of 15-25 μm. The P^+ floating layers are then incorporated into this drift region using buried multi-epitaxial growth process[18]. The buried P^+ floating layers thickness and width can be fixed within 1-3 μm. Since the P^+ floating layers needs to have channels connecting the upper and lower drift regions, these must be of either stripe or dot pattern. The dotted pattern is more effective than the striped pattern for the improvement in the on-resistance[18]. These floating layers are formed by an *n*-layer growth at a substrate temperature of 1000 ºC by chemical vapour deposition (CVD) using SiH_4 gas where *n* is the number of P^+ buried floating layers. The thickness and doping concentration of these buried P^+ floating layers have to be kept equal to the first epitaxial layer. After these, P^+ floating layers are fabricated, the surface *p*-guard rings are required to be formed using boron ion-implantation followed by annealing. Once the P^+ floating buried layers are fabricated along with the surface *p*-guard rings, the device active area is to be defined using wet chemical etching of thermally grown SiO_2. An approximately 1.5 μm deep P-base region is to be diffused by boron implantation followed by activation to obtain an electrically active boron surface concentration of 1.0×10^{17} cm^{-3}. The windows are then opened by etching thermally grown SiO_2 and gate is defined followed by formation of gate oxide (800-600Å). Boron ions are then implanted into the channel region for the FLIMOSFET body. Polysilicon deposition is then carried out by CVD to form the gate electrode. Once the gate is patterned, arsenic ions are implanted to form the FLIMOSFET N^+ source region of about 0.2 μm deep. The last step is the metallization. A phosphorous-doped oxide is deposited over the entire wafer followed by heating the wafer to give a smooth surface topography. Contact windows are defined and etched, followed by depositing and patterning a metal layer, such as aluminium to form ohmic contacts from source and drain regions.

Results and Discussion

To understand the behaviour of the proposed device we started with the simulation of a 2-dimensional device structure of (4 μm × 25 μm) dimensions respectively as shown in Fig. 2. The doping densities were chosen to simulate a typical power MOSFET. We then implanted P^+ floating islands in the N^-drift region one-by-one up to eleven. The device was then studied both under on/off states and results were obtained with the FLIMOSFET structure by varying the number of P^+ floating islands one-by-one and then keeping them fixed at eleven.

The on-state of the device means when the V_g becomes greater than the V_T, i.e., the threshhold voltage of the device. It is observed that the flow of carriers starts once the V_g becomes greater than the V_T. Fig. 3 shows the channel formation in the on-state at V_g = 5 V, which is required to validate the device operation in the on-state. As long as there is no channel formation, no current conduction can take place. Further, Fig. 3 also suggests that the device has an approximate value of threshold voltage V_T = 5 V. The on-state behaviour of the device can be further explored with the help of Fig. 4, which shows the current flow lines, which indicate the current path through the device in its on-state. Fig. 4 shows that the current flow path almost remains unaffected with the incorporation of these floating islands and it resembles the current path of a conventional power MOSFET, whereas the current densities are also not much reduced and the device behaves in a normal manner as the conventional power MOSFET would have done in terms of current flow.

Figure 5 shows the PISCES-simulated electric field distribution under the off-state conditions in the drift region by varying the doping concentration in this

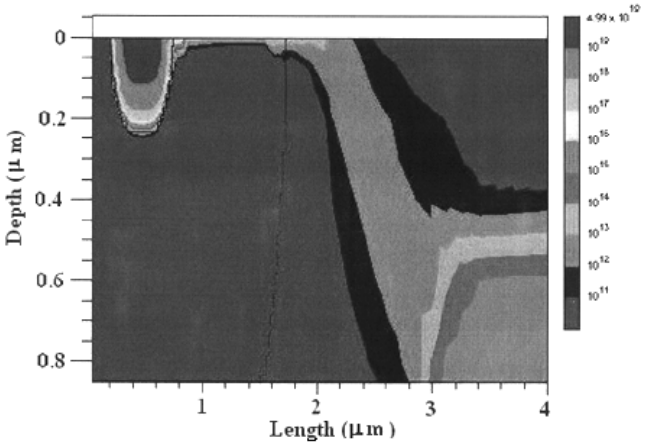

Fig. 3 — PISCES simulated 2D plot showing channel formation in the on-state at V_{gs} = 5 V

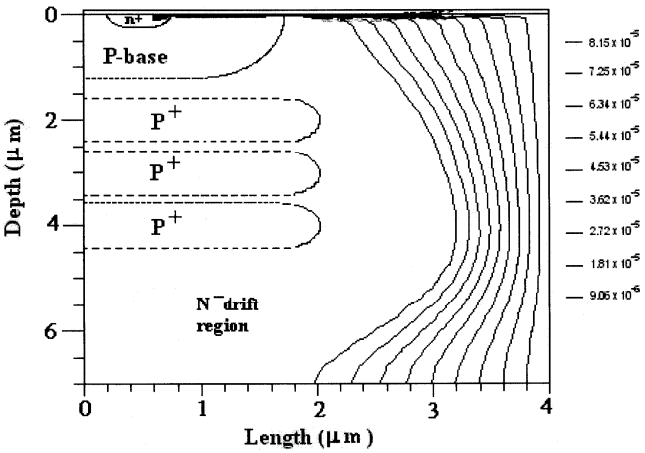

Fig. 4 — PISCES simulated 2D plot showing current flow lines in the on-state at V_{gs} = 12 V and V_{ds} = 25 V

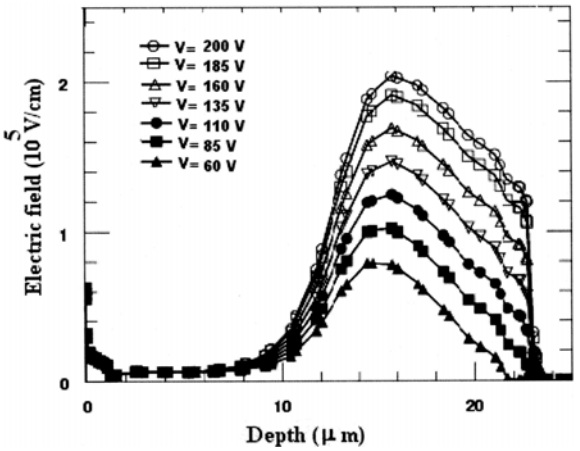

Fig. 6 — Electric field distribution in the off-state with increasing drain bias

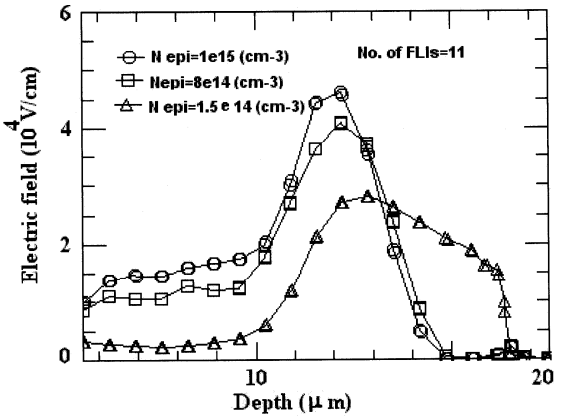

Fig. 5 — Electric field distribution in the off-state with various drift region doping levels at V_{ds}=25 V

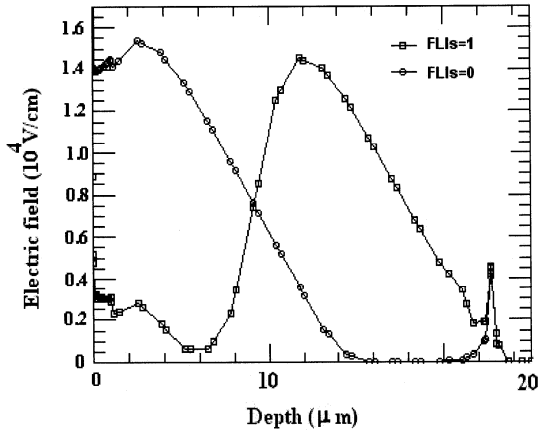

Fig. 7 — Electric field distribution in the off-state by varying the number of floating islands

region at a fixed drain potential of 25 V, keeping the floating islands equal to eleven. It is observed that the electric field gets lowered with the decrease in the doping concentration in the drift region of the device. Since the value of the electric field ranges much lower than the critical electric field given by those of the silicon devices (~3 × 10^5 V/cm), the doping of the drift region could be enhanced as long as the electric field remains less than the critical electric field. Hence, the reduction in the on-resistance of the device takes place by a factor equivalent to the enhancement in doping of the drift region as given by the standard equation $R_{ON,\,sp} = W_T / q\ \mu_n N_D$, where W_T is the width, μ_n is the electron mobility and N_D is the doping of the drift region, respectively. It is observed that there exists a non-linear relationship in the electric field reduction with the decrease in the drift region doping. Fig. 6 shows another useful PISCES simulated plot showing electric field variations with increasing drain bias in the drift region in the off-state. This plot suggests that the electric field tends to increase with the increase in the drain bias and the field profile is triangular with almost constant slope and advancing towards the N^+ drain contact, as the applied voltage increases since the depletion region expands gradually as the voltage increases. The field profiles for larger voltages have relatively flat shape with steep variations only near the contacts. It is observed that the electric field is vertical and its value is the maximum at the junctions. The breakdown voltage is simply the area under the field profile, when the maximum field reaches a critical value. Therefore, the key idea is to keep the maximum field below its critical value as already mentioned above. Fig. 7 shows the effect on the peak electric field by incorporating a floating island in the conventional structure. It is observed that a single floating island reduces the peak electric field by about 4% in the off-

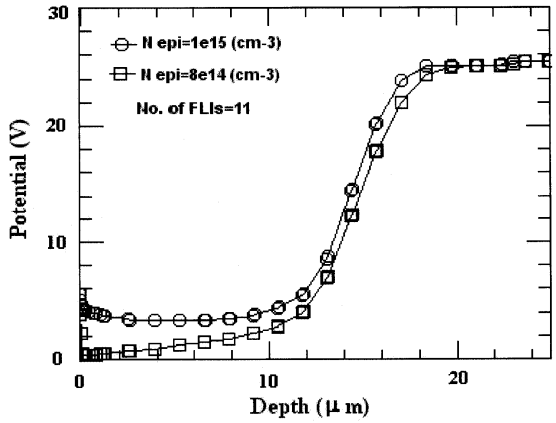

Fig. 8 — Potential distribution in the on-state for various doping levels

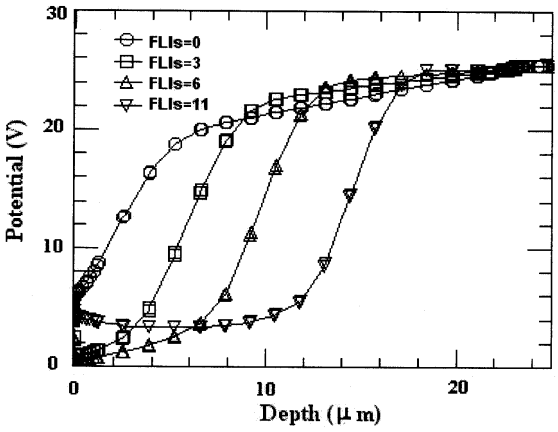

Fig. 9 — Potential variations in the on-state by varying the number of floating islands

state within the drift region of the device which is a key feature of this device.

Figure 8 shows the potential distribution in the on-state with in the drift region of the device at gate potential equal to 5 V and drain potential equal to 25 V with eleven floating islands added one-by-one. It is observed that the intermediate potential of the device with floating islands tends to decrease with the reduced drift region doping concentration, which is required. It is evident from this figure that the intermediate potential is less throughout the whole drift region for reduced doping. Fig. 9 shows the potential distribution in the on-state in the drift region for V_{gs} = 5 V and V_{ds} = 25 V by varying the floating islands from 0 to 11. It is observed that there is a reduction in the intermediate potential within the drift region with the increase in the floating islands, which is desired. Therefore, it is concluded that the drift region doping and number of floating islands play an important role in the FLIMOSFET in lowering the

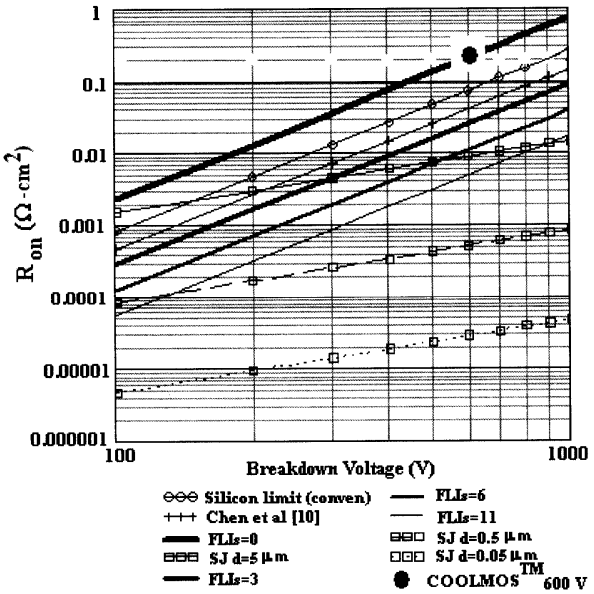

Fig. 10 — On-resistance versus breakdown voltage comparison for various modern power devices.

maximal electric field in the drift region of the device and intermediate potential, thereby reducing the on-resistance of the device quite effectively without causing any noticeable changes in the device performance.

Finally, Fig. 10 shows a comparison of the on-resistance versus breakdown voltage for the various modern power devices. These curves are based on the analytical calculations based on the available literature. It is shown that there is a trade-off in the on-resistance versus breakdown voltage design and the power FLIMOSFETs can break the conventional silicon limit.

Conclusions

A power FLIMOSFET device structure has been discussed both in on/off states with the help of various internal electrical quantities such as electric field and potential distribution based on the device simulation results obtained using PISCES-IIB. It is observed that in this device, electric field and intermediate potential distribution in the drift region tend to decrease with the decrease in the drift region doping and with the increase in number of floating islands. The doping concentration could be enhanced as long as the electric field remains less than its critical value for silicon devices. Thus, the FLIMOSFET structure is very attractive because it gives reduced on-resistance (R_{on}) as compared to the conventional VDMOSFET. The device structure does not require any precise control of the boron implantation dose in the P^+

floating islands for charge balance as essential in case of super junction (SJ)/COOLMOS^{TM} devices. The process flow mechanism required to fabricate FLIMOSFET structure using multi-epitaxial technology has been discussed for the first time, which is less complex and less expansive than the super junction (SJ) devices technology.

Acknowledgement

One of the authors (RV) gratefully acknowledges Prof. S K Khosa, Head, Department of Physics & Electronics, University of Jammu, for his constant encouragement throughout this work and the University Grants Commission (UGC), Govt. of India, for the award of 'Teacher Fellowship' under the FIP scheme during the 10th plan period. The authors also wish to acknowledge Mr. Rockey Gupta, Department of Physics & Electronics, University of Jammu, and Mr. K. Narasimhulu, Department of Electrical Engineering, IIT Bombay, Mumbai, for fruitful discussions.

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