Analog multiplier using operational amplifiers

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Simple circuit technique for implementing four-quadrant analog multiplier has been presented. The proposed circuit requires only operational amplifier (opamp) as the active element. The realization method is based on the quarter-square technique where a square is provided from the inherent quadratic behaviour of class-AB output stage of opamp. Experimental results showing the circuit performance are described. The worst-case linearity error and total harmonic distortion for maximum operating range are about 0.23 and 1.02%, respectively.

Keywords: Analog multiplier, Opamp, Quarter-square technique, Squaring circuit, Class AB configuration

1 Introduction

Analog multiplier is an important circuit building block in the field of analog signal processing. Its applications can be found in communication, measurement and instrumentation systems. In the past, analog multiplier based on a variable transconductance technique is proposed. Many commercial analog multipliers using this technique are available in the form of integrated circuit fabricated in bipolar technology. Alternately, one of the successful techniques to realize an analog multiplier is based on the use of quarter-square technique. The squaring schemes of current input signal can be performed using translinear principle. However, these schemes realized for the specific purpose are unavailable in the commercial integrated circuit form. It is known that output stage of a general-purpose opamp is a class-AB configuration. The characteristic of a class-AB configuration can be expressed by the translinear principle and exploited to realize a high performance squaring scheme. The square operation achieved by this mention is suited for the realization of analog multiplier using quarter-square technique. The use of an opamp in the realization of analog multiplier will provide the structure of high performance at low cost and simple construction. In this paper, four-quadrant analog multiplier is described. The proposed circuit requires only opamp as the active elements. Experimental results that verify the circuit performance will be given.

2 Circuit Description

The proposed analog multiplier is shown in Fig. 1. The circuit operation can be expressed as follow. Assuming that opamps $A_1$ and $A_2$ are well matched such as $I_{B1} = I_{B2} = I_B$ and $I_{S1} = I_{S2} = I_S$, where $I_B$ and $I_S$ denote the quiescent current and class-AB bias current of opamp, respectively. Opamps $A_1$ and $A_2$ and resistors $R_{S1} - R_{S2}$ form an unity gain summing amplifier with supply current sensing. Resulting voltage $v_{11}$ and $v_{12}$ are, respectively, sum and difference of input voltage $v_x$ and $v_y$. Resistors $R_{11}$ and $R_{12}$ convert the signal voltages $v_{11}$ and $v_{12}$ into the signal currents $i_{11}$ and $i_{12}$. For the output currents $i_{11}$ and $i_{12}$ less than $2I_S$, the quadratic characteristic of class-AB output stage of opamps $A_1$ and $A_2$, which exist in the supply currents $I_1$ and $I_2$, are fulfilled.

The supply currents $I_1$ and $I_2$ are sensed and converted to voltages $v_{21}$ and $v_{22}$ by resistors $R_{21}$ and $R_{22}$, respectively. If resistors $R_{11} = R_{12} = R_C$, $R_{21} = R_{22} = R_S$, $R_{S1} = R_{S2} = R_S = R_m$ and $R_{21} = R_{22}/2$ are assigned, then voltages $v_{21}$ and $v_{22}$ can be written as:

$$v_{21} = v_{CC} - (I_B + I_s)R_{21} - \frac{v_{11}^2R_{21}}{8I_S^2R_{11}^2} - \frac{v_{11}R_{21}}{2R_{11}} \text{ for } \frac{v_{11}}{R_{11}} \leq 2I_S$$

$$v_{22} = v_{CC} - (I_B + I_s)R_{22} - \frac{v_{12}^2R_{22}}{8I_S^2R_{12}^2} - \frac{v_{12}R_{22}}{2R_{12}} \text{ for } \frac{v_{12}}{R_{12}} \leq 2I_S$$

Voltages $v_{21}$ and $v_{22}$ will transfer to four input difference amplifier formed by opamp $A_3$ and resistors $R_{31} - R_{6}$, where $R_3 = R_6 = R_p$, $R_1 = R_4 = R_1$ and $R_2 = R_5 = R_q$. From routine circuit analysis, voltages $v_{11}$ and $v_{12}$
are, respectively, sum and difference of input voltages $v_x$ and $v_y$. Therefore, the output voltage $v_o$ can be stated as:

$$v_o = \frac{R_i R_s}{2 R_c R_q I_s} v_x v_y + 2 \left( \frac{R_s}{2 R_c} - \frac{R_i}{R_p} \right) v_y \quad \ldots(3)$$

To provide the multiplication operation, the condition of $R_d/R_q = R_s/2R_c$ is assigned. Hence the output voltage can be expressed as:

$$v_o = \frac{R_i R_s}{2 R_c^2 R_q I_s} v_x v_y = -k_m v_x v_y \quad \ldots(4)$$

where $k_m$ denotes the multiplication gain. From Eq. (4), it can be seen that four-quadrant analog multiplier can be simply realized using general purpose opamp without specific device.

3 Circuit Performance

Deviation from ideal performance of the proposed circuit is disturbed by the mismatches between opamps $A_1$ and $A_2$ and the tolerance of resistors being used. The device mismatches will influence the multiplication gain error and second harmonic distortion of the input signals $v_x$ and $v_y$. The output voltage $v_o$ included term of errors and can be expressed as:

$$v_o = -\frac{R_i}{R_c} \left( (1 + \varepsilon_1) v_x v_y + \varepsilon_2 v_x^2 + \varepsilon_3 v_y^2 \right) + \varepsilon_4 \quad \ldots(5a)$$

$$\varepsilon_1 = 4\Delta - \frac{6R_q}{R_f} \Delta + \Delta_s \quad \ldots(5b)$$

$$\varepsilon_2 = 3\Delta - \frac{3R_q}{R_f} \Delta + \frac{\Delta_s}{2} \quad \ldots(5c)$$

$$\varepsilon_3 = 4\Delta - \frac{3R_q}{R_f} \Delta + \frac{\Delta_s}{2} \quad \ldots(5d)$$
$v_{\text{off}} = (I_{B1} - I_{B2} + \Delta_s)(1 + 2\Delta) \frac{R_S}{R_q} \quad \text{...(5e)}$

where $\Delta$ is the tolerance of resistors, $\Delta_s = (I_{S1} - I_{S2})$ is the mismatch between class-AB bias currents of opamps $A_1$ and $A_2$, $\varepsilon_1$ to $\varepsilon_3$ and $v_{\text{off}}$ denote the error factors and offset voltage, respectively. If $R_1/R_q = 1$, $\Delta = 1 \times 10^{-3}$, $\Delta_s = 1.3 \times 10^{-6}$, $I_{B1} = 0.537$ mA, $I_{B2} = 0.539$ mA, then errors $\varepsilon_1$ to $\varepsilon_3$ are calculated as $\varepsilon_1 = 2 \times 10^{-4}$, $\varepsilon_2 = 1.3 \times 10^{-6}$, $\varepsilon_3 = 1 \times 10^{-3}$ and $v_{\text{off}} = 6.6$ mV. The input operating range of the proposed circuit can be considered from the accepted value of the output current drawn from opamps $A_1$ and $A_2$ to fulfill the condition in Eqs (1) and (2). The voltages $v_{21}$ and $v_{22}$ included higher-order terms can be expressed as:

$$v_{21} = V_{CC} - I_{B1} R_{21} - I_{S1} R_{21} + \frac{V_{S1}^2}{8 I_{S1}^2 R_{21}^2} - \frac{V_{S1}^4}{128 I_{S1}^4 R_{21}^4} + \ldots$$

$$v_{22} = V_{CC} - I_{B2} R_{22} - I_{S2} R_{22} + \frac{V_{S2}^2}{8 I_{S2}^2 R_{22}^2} - \frac{V_{S2}^4}{128 I_{S2}^4 R_{22}^4} + \ldots$$

4 Experimental Details

The proposed circuit in Fig. 1 was constructed using commercially available opamps UA741 and 0.1% tolerance resistors. The resistors used in the circuit are chosen to be $R_{21} = R_{22} = 5 \Omega$, $R_{31} = R_{32} = 2 \Omega$, $R_3 = R_4 = R_5 = R_{31} = R_{32} = R_{41} = R_{51} = R_{52} = 100 \Omega$, $R_{42} = 500 \Omega$ and $R_3 = R_6 = 500 \Omega$. The power supply voltages used were set to ±9V. The quiescent currents and the class-AB bias currents of opamps $A_1$ and $A_2$, respectively, were measured as $I_{B1} = 0.537$ mA, $I_{B2} = 0.539$ mA, $I_{S1} = 144.8$ µA and $I_{S2} = 146.1$ µA using the technique proposed earlier. Hence scale factor $k_m$ and input operating range can be calculated as 0.275 and ±0.91 V, respectively. The measure of $dc$ transfer characteristic is shown in Fig. 2. Figure 3 shows the linearity error for input voltage $v_x$ varied from −1V to 1V and $v_y = 0.5$ V. For input operating range, $|v_x| + |v_y| = 0.9$ V, the worst-case linearity error of Fig. 3 is about 0.9 mV or
relative error of 0.23% for input voltage $v_x$ of −0.4V. The output response of the proposed circuit can be investigated from the total harmonic distortions (THDs). The measure of THDs is determined by applying a sinusoidal wave to $v_x$ and dc voltage varied from −1 V to 1 V to $v_y$. Figure 4 shows THDs versus input voltage $v_x$ at 1, 10 and 50 kHz of peak amplitude 100 mV. Figure 5 shows the result of amplitude modulation for 20 kHz sinusoidal wave of 0.4 V peak amplitude and 1 kHz triangular wave of 0.2 V peak amplitude applied to $v_x$ and $v_y$, respectively. It is clearly seen that the proposed circuit provides an adequate performance of analog multiplier.

5 Conclusions
Four-quadrant analog multiplier using opamps as only active element has been described. The realization method is based on opamp supply current sensing to provide the squaring of sum and difference of two input signals for quarter-square algebraic identity. The proposed circuit provides a simple construction, a good performance and low cost. Experimental results show that the proposed circuit exhibits basic feature of multiplier for analog signal processing.

References