Single DC source H-bridge topology as a low cost multilevel inverter for marine electric systems

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This paper proposes a new design and analysis of Single DC Source H-bridge inverter (SDSI) topology as a multilevel inverter to reduce the cost, installation space of marine electric systems. This new design converts the SDSI into a buck converter (BC) and multilevel inverter (MLI). The newly designed single DC source multilevel inverter (ND-SDCMI) does not require a change its structure and blocking voltage to create n numbers of levels. The ND-SDCMI is compared with existing single DC source multilevel inverter (SDCMI) topologies in terms of the number of levels of output voltage, blocking voltage, switching devices, total harmonic distortion (THD), and other components. Simulation results of THD, efficiency, blocking voltage, and output voltage for a 12-level ND-SDCMI are discussed in detail. Prototype 12-level ND-SDCMI is implemented and programmed using a relatively inexpensive F28027 microcontroller.

[Keywords- Buck converter, multilevel inverter, single DC source multilevel inverter]

Introduction
Multilevel inverters have been used in electric propulsion system, power quality improvement systems for marine application. Multilevel inverters (MLIs), which constitute a new class of power inverters in the field of power electronics, offer several advantages over 2-level inverters, such as high power quality, low switching loss, and high voltage application. The cost, power quality, efficiency, installation space, complexity, and reliability are the key factors for the selection of the MLI for marine electric system. A 3-level MLI has been reported initially to increase the power quality. In the conventional topologies of MLIs, the cascaded H-bridge multilevel inverter (CHBMLI) is more advantageous than the diode clamped MLI (DCMLI) and flying capacitor MLI (FCMLI) because it has a modular structure and low electromagnetic interference (EMI). Furthermore, CHBMLI does not require any clamping diodes and capacitors unlike the DCMLI and FCMLI, respectively.

The primary issue with the CHBMLI is that it requires different DC sources for each H-bridge. The large number of DC sources increases the cost and installation space of the CHBMLI. Moreover, the large number of DC sources affect the reliability and efficiency of the MLI. To solve this issue of the CHBMLI, a single DC source CHBMLI has been used with single-phase and three-phase transformers. However, the presence of a transformer increases the complexity, installation space and cost. A toroidal transformer with a high-frequency link has been used for an asymmetrical MLI to reduce the number of transformers. The demerits of this topology are that it uses an extra unit of AC/DC or DC to DC converter, number of H bridges, and capacitors.

To overcome these demerits, a transformer-less topology of SDCMI was proposed using an AC to DC converter, filters and isolators. This topology required a large number of passive components, thereby decreasing its reliability. Recently, a transformer-less buck converter (BC) based H-bridge topology was implemented to obtain variable DC voltage from a single DC source. The disadvantage of this topology is that it requires an additional BC unit. Unfortunately, the major drawbacks of the aforementioned topologies are the installation space, cost, complexity, losses, inadequate control, and low reliability. A new design or topology is required to overcome the aforementioned demerits.

The conventional SDSI has been described using an H-bridge with an LC filter as depicted in Fig. 1. The H-bridge generates a 3-level output voltage and the LC filter reduces the harmonics from the 3-level...
Voltage waveform. This paper proposes a new design and analysis for the conventional SDSI depicted in Fig. 1. The new design converts the conventional SDSI into a BC; it creates a positive and negative voltage from a single DC source by suitable control of the duty cycle. The values of the duty cycle, inductor, and capacitor have been selected to create \( n \) number of levels in the output voltage of ND-SDCMI. The ND-SDCMI offers numerous advantages in terms of size, complexity, installation space, number of components, and blocking voltage over the existing SDCMI.

### Materials and Methods

**New Design of SDSI**

The circuit diagram of the conventional SDSI is depicted in Fig. 1. The circuit consists of a single DC source, an H-bridge, an inductor, and a capacitor. Basically, the proposed design enables an SDSI to function as a BC, which, by suitable design and control of the duty cycle, can be converted into an MLI. The design and operation of the SDSI as BC or MLI is discussed in next section.

The topology works in two modes as a BC. The two operational modes are described in TABLE 1.

![Fig. 1 — Structure of the SDSI](image)

Table 1 presents the current flowing through the circuit and load voltage for operational modes I and II and for \( D > 0.5 \), \( D < 0.5 \). The analysis has been described below:

In mode I, the voltage across the inductor increases as given in Eq. (1).

\[
V_L = L \frac{di}{dt}
\]

\[
\Delta i = \frac{V}{L} \frac{T_{ON_{S11,S14}}}{T_{OFF_{S11,S14}}}
\]

By applying Kirchhoff’s voltage law to mode I, Eq. (3) is obtained

\[
V_{in} = V_L + V_{RL} + 2V_Q
\]

Substituting the Eq. (3) in (2), we can obtain the rate of rise of current in the circuit given by Eq. (4).

Rate of rise of current

\[
\Delta i(+) = \frac{V_{in} - V_{RL} - 2V_Q}{L} \frac{T_{ON_{S11,S14}}}{T_{OFF_{S11,S14}}}
\]

By applying Kirchhoff’s voltage law to mode II, Eq. (5) is obtained

\[
V_L = V_{in} + V_{RL} + 2V_Q
\]

Now, substituting Eq. (5) in (2), the rate of decrease of current, when the inductor is discharged can be written as Eq. (6).

Rate of decrease of current

\[
\Delta i(-) = \frac{V_{in} + V_{RL} + 2V_Q}{L} \frac{T_{OFF_{S11,S14}}}{T_{ON_{S11,S14}}}
\]

To obtain the load voltage, \( V_{RL} \) as a function of the duty cycle \( D \), Eqs. (4) and (6) are equated as follows:

\[
V_{RL} = \left[ \left( V_{in} + 2V_Q \right) \frac{T_{OFF_{S11,S14}}}{T_{ON_{S11,S14}} + T_{OFF_{S11,S14}}} \right] + \left( -V_{in} + 2V_Q \right)
\]

The duty cycle is defined by Eq. (8)

\[
D = \frac{T_{ON_{S11,S14}}}{T_{ON_{S11,S14}} + T_{OFF_{S11,S14}}}
\]

After substituting Eq. (8) in (7), the load voltage and load current are given by Eq. (9) and (10), respectively: Load voltage

\[
V_{in} = \left( V_{in} + 2V_Q \right) \frac{T_{OFF_{S11,S14}}}{T_{ON_{S11,S14}} + T_{OFF_{S11,S14}}} + \left( -V_{in} + 2V_Q \right)
\]

\[
I_{RL} = \left( V_{in} + 2V_Q \right) \frac{T_{OFF_{S11,S14}}}{T_{ON_{S11,S14}} + T_{OFF_{S11,S14}}} + \left( -V_{in} + 2V_Q \right)
\]
$V_{RL} = V_{in} (2D - 1) - 2V_Q \quad \ldots (9)$

Load current

$$i_{RL} = \frac{V_{RL}}{R_L} \quad \ldots (10)$$

From Eq. (9) and (10), when $D$ is greater than 0.5, the load voltage and current are positive. Furthermore, if $D$ is less than 0.5, the load voltage and load current are negative. The newly designed buck converter produced a different magnitude of load voltage ranging from $-V_{in}$ to $+V_{in}$ by varying the duty cycle from 0 to 1.

Design of the SDSI as an SDCMI

The ND-SDCMI can be explained in following steps:

**Step 1:** Find the value of the duty cycle to create the desired number of levels in the load voltage

The load voltage, which depends upon the duty cycle is given by Eq. (9). The load voltage of the BC is modified to create $n$ number of levels in the output voltage. The modified equation that converts the BC into an MLI is given by Eq. (11). The number of duty cycles required to create $n$ number of levels is $d = n-1$ (for odd $n$), $d = n$ (for even $n$).

$$V_{RL_m} = V_{in} (2D_m - 1) - 2V_Q \quad \ldots (11)$$

$m = 1$ to $n-1$ for odd $n$

$m = 1$ to $n$ for even $n$ (when zero level is not considered)

Figure 2 shows the 13 level load voltage as per Eq. 11. To create 13 levels, $d = 12$, $m = 1$ to 12 and the 12 different values of $\theta$ are required, as shown in Fig. 2. The duty cycle $D_m$ is constant for the period $\theta_{n-1} - \theta_n$.

**Step 2:** Define the minimum and maximum output power of ND-SDCMI

$$P_{out\ max} = V_{RL\ max} I_{RL\ max} \quad \ldots (12)$$

$$P_{out\ min} = V_{RL\ min} I_{RL\ min} \quad \ldots (13)$$

**Step 3:** Determine the value of load resistance of ND-SDCMI

$$R_{L\ max} = \frac{V_{RL\ max}}{I_{RL\ max}} \quad \ldots (14)$$

$$R_{L\ min} = \frac{V_{RL\ min}}{I_{RL\ min}} \quad \ldots (15)$$

**Step 4:** Select the number of levels ($n$) in the output voltage and hence determine the minimum value of the inductor

Let the output frequency of ND-SDCMI be $F = \frac{1}{T_F}$

The settling time of the load voltage, $V_{RL_m}$ at any duty cycle is, $T_s = \frac{4L}{R_L 4n}$

$$T_s \leq \frac{T_F}{n} \quad \text{or} \quad \frac{4L}{R_{L\ min}} \leq \frac{T_F}{n} \quad \ldots (16)$$

The minimum value of inductor of the ND-SDCMI

$$L_{min} \leq \frac{T_F R_{L\ min}}{4n} \quad \ldots (17)$$

The settling time of the output voltage of the ND-SDCMI is given by Eq. (16). Equation (16) must be satisfied to create $n$ levels of output voltage. To satisfy this condition, the value of $L_{min}$ is calculated using Eq. (17).

If the value of $\theta_m$ is known, as shown in Fig. (2), the value of inductor can be calculated.

$$T_s \leq \theta_{m+1} - \theta_m \quad \text{Here } m = 1 \text{ to } n-1 \quad \ldots (18)$$

So

$$\frac{4L}{R_{L\ min}} \leq \theta_{m+1} - \theta_m \quad \text{or}$$

$$L \leq \frac{R_{L\ min} (\theta_{m+1} - \theta_m)}{4L} \quad \ldots (19)$$

The other method determines the value of the inductor using Eq. (18) and Eq. (19). In this paper, the value of the angles of output voltage $\theta_m$ has been calculated by comparison of multilevel waveform steps with the sinusoidal wave depicted in Fig. 2.
Step 5: Determine the minimum value of filter capacitor using Eq. (20).

\[
C_{\text{min}} \leq \frac{V_{\text{fL}} \max (1 - V_{\text{fL}} \max)}{8L_s^2} \quad \text{... (20)}
\]

The cost of semiconductor switches depends upon the blocking voltage and number of semiconductor devices used in a topology. The maximum blocking voltage of the H-bridge based MLI has been calculated. Maximum blocking voltage of ND-SDCMI was calculated using Eq. (21).

\[
V_{\text{block}} = 4V_{\text{in}} = V_{\text{block}1} + V_{\text{block}4} + V_{\text{block}2} + V_{\text{block}3} \quad \text{... (21)}
\]

In this topology S11 and S14 work together while S12 and S13 work simultaneously. The blocking voltage for the ND-SDCMI can be written using Eq. (22).

\[
V_{\text{block}1} = V_{\text{block}4} \text{ or } V_{\text{block}2} = V_{\text{block}3} \quad \text{... (22)}
\]

By substituting Eq. (22) in Eq. (21), the maximum blocking voltage is given by Eq. (23).

\[
V_{\text{block}} = 2(V_{\text{block}1} + V_{\text{block}2}) = 2(V_{\text{block}3} + V_{\text{block}4}) \quad \text{... (23)}
\]

The THD is calculated using the MATLAB/SIMULINK-FFT toolbox as the number of levels increases in the output voltage. The THD of output voltage of the ND-SDCMI is given in Eq. (24)

\[
THD = \sqrt{\sum_{n=2}^{\infty} \frac{v_n}{v_1}} \quad \text{... (24)}
\]

The blocking voltage of the ND-SDCMI depends upon the input voltage given in Eq. (21). Figure 3 depicts that the blocking voltage remains constant when \( n \) number of levels are created, which also indicates that the cost of the semiconductor device of the ND-SDCMI is independent of the THD or number of levels in the load voltage. If the number of levels in load voltage increases, the THD decreases. Therefore, the basic advantage of the new designed topology is that the overall cost of the proposed ND-SDCMI remains constant despite an increase in the power quality of the output voltage.

The efficiency of the ND-SDCMI is calculated using Eq. (25). The analysis of the switching losses, conduction losses of semiconductor devices, and conduction losses of diodes of the ND-SDCMI is performed using MATLAB/Simulink.

The output power (Pout) and input DC voltage (Vin) are assumed to be 1 kW and 200 V, respectively. The switching time, RON and diode forward voltage are calculated using the MOSFET IRF640 datasheet. The analysis of the efficiency is performed by substituting power losses in Eq. (25) when the duty cycle varies from 0 to 1 as shown in Fig. 4(a). Figure 4(a) shows that the maximum efficiency of the ND-SDCMI is 98.57% and 99.58% at the minimum and maximum duty cycle, respectively. The selection of the duty cycle improves the efficiency. The efficiency varies from 98% to 92% when the duty cycle varies from 0 to 0.45 and from 99% to 94% when the duty cycle varies from 1 to 0.55, as depicted in Fig. 4(a). If the duty cycle of the ND-SDCMI operates from 0 to 0.45 and from 0.55 to 1, the losses are minimum and the efficiency improves. The duty cycles are selected and the efficiency and THD are calculated up to 13 levels as depicted in Fig. 4(b).

Figure 4(b) shows that the maximum efficiency of the ND-SDCMI is 99.5% for two levels; however, when the number of levels in the output voltage increases, the efficiency marginally decreases. Figure 4(b) shows that to obtain a THD less than 5% of the fundamental voltage, ND-SDCMI requires at least

![Fig. 3 — THD and blocking voltage obtained by simulation as the number of levels increases in the output voltage (V_{\text{in}} = 12 V)](image-url)
12 levels in the output voltage. The efficiency for 12-level ND-SDCMI is 94%. From Fig. 4 and the above discussion, an improvement in THD appears to be accompanied by a marginal decrease in the efficiency of the ND-SDCMI.

Comparison of reported topology of an SDCMI with that of the ND-SDCMI

Table 2 shows the comparison of an SDCMI with the ND-SDCMI. A comparative analysis shows that, when one H-bridge is used, that is, \( h = 1 \), the ND-SDCMI has less blocking voltage (48 V) to create \( n \) number of levels. Table 2 shows that blocking voltage is calculated for the number of H-bridges used in a single-phase SDCMI topology. The THD of the output voltage of the SDCMI is below 5%. According to the IEEE-519 or IEC 555-2 standard, the THD in the output voltage should be less than five percent

When only one H bridge is used (\( h = 1 \)), only three topologies have a THD less than 5%. From Table 2, when THD is below 5%, ND-SDCMI and the topologies reported in ref. [15] and [22] require only four semiconductor devices; whereas, other topologies require a larger number of semiconductor devices. The ND-SDCMI uses a smaller number of components than existing topologies do. Therefore, the ND-SDCMI requires less installation space and costs less than existing topologies do.

![Fig. 4 — Efficiency and THD of the ND SDCMI.](image)

**TABLE 2 — Comparison of different parameters of an ND-SDCMI with reported SDCMI, when \( h = 1 \)**

<table>
<thead>
<tr>
<th>Ref.</th>
<th>( V_{\text{block}} ) in volts</th>
<th>No. of levels</th>
<th>No. of levels shown in reported study</th>
<th>No. of switches</th>
<th>THD for ( h = 1 )</th>
</tr>
</thead>
<tbody>
<tr>
<td>[22]</td>
<td>( &gt;4 \ V_{dc} ) ( h = 1 )</td>
<td>( &gt;48 )</td>
<td>3</td>
<td>3</td>
<td>4</td>
</tr>
<tr>
<td>[14]</td>
<td>( (4 \ V_{dc}) h )</td>
<td>48</td>
<td>( 3^h )</td>
<td>3</td>
<td>27</td>
</tr>
<tr>
<td>[10]</td>
<td>( (4 \ V_{dc}) h )</td>
<td>48</td>
<td>( 2h+1 )</td>
<td>3</td>
<td>13</td>
</tr>
<tr>
<td>[13]</td>
<td>( \left(4 \ V_{dc} \right) \left(\frac{V_{dc}}{9}\right) )</td>
<td>48</td>
<td>( 3^h )</td>
<td>3</td>
<td>27</td>
</tr>
<tr>
<td>[3]</td>
<td>( &gt;4 V_{dc} ) ( h = 1 )</td>
<td>( &gt;48 )</td>
<td>-</td>
<td>3</td>
<td>5</td>
</tr>
<tr>
<td>[15]</td>
<td>( &gt;4 V_{dc} ) ( h = 1 )</td>
<td>( &gt;48 )</td>
<td>( n )</td>
<td>( n )</td>
<td>3 to 255</td>
</tr>
<tr>
<td>[12]</td>
<td>( &gt;4 (4 V_{dc}) h )</td>
<td>( &gt;48 )</td>
<td>( 3^h )</td>
<td>3</td>
<td>upto 27</td>
</tr>
<tr>
<td>[4]</td>
<td>( (4 V_{dc}) h )</td>
<td>48</td>
<td>( 2h+1 )</td>
<td>3</td>
<td>7</td>
</tr>
<tr>
<td>[4]</td>
<td>( (4 V_{dc}) h )</td>
<td>48</td>
<td>( 2h+1 )</td>
<td>3</td>
<td>7</td>
</tr>
<tr>
<td>[11]</td>
<td>( (4 V_{dc}) h )</td>
<td>48</td>
<td>( 2h+1 )</td>
<td>2T+1</td>
<td>7</td>
</tr>
<tr>
<td>[24]</td>
<td>( &gt;4 V_{dc} ) ( h = 1 )</td>
<td>( &gt;48 )</td>
<td>5</td>
<td>-</td>
<td>5</td>
</tr>
<tr>
<td>[23]</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>5</td>
</tr>
<tr>
<td><strong>ND-SDCMI</strong></td>
<td>( (4 V_{dc}) )</td>
<td>48</td>
<td>( n )</td>
<td>( n )</td>
<td>13</td>
</tr>
</tbody>
</table>
Table 3 shows the comparison of a single DC source topology when THD is less than 5% of the fundamental voltage. From Table 3, when THD is less than 5% and input DC voltage is 12 V, the ND-SDCMI generates 13 output levels. The blocking voltage is 48 V, which is less than that of existing topologies. Table 3 shows that apart from semiconductor devices, the other topologies require transformers, which are heavy to install and require two or more passive devices. The ND-SDCMI, however, requires only an inductor and capacitor to perform multilevel operations.

**Results and Discussion**

Figures 5(a) and 5(b) depict the 12-level output voltage and current of the ND-SDCMI when a resistive load has been connected. The voltage across the inductor of a 12-level ND-SDCMI is depicted in Fig. 5(c).

Figure 5(d) depicts the blocking voltage across switches $S_{11}$ and $S_{14}$. The blocking voltage across $S_{12}$ and $S_{13}$ is shown in Fig. 5(e). From the simulation results we analyzed that the maximum blocking voltage of the ND-SDCMI is 48 V when $V_{\text{in}}=12$ V. Figure 6 depicts that the THD of the load voltage of the ND-SDCMI is 4.6%, and the rms value of load voltage is 8 V.

The experimental results are validated with simulation results by the implementation of the prototype 12-level ND-SDCMI. The same parameters that were selected for the simulation (Table 4) were selected for experimental work. The IRF-640 MOSFET device is used for the H-bridge and the gate driver TLP250 is used to drive the MOSFET device. The look-up table of the duty cycle has been
The output voltage, voltage across inductor, and gate signal of H-bridge obtained using the microcontroller are measured using a mixed signal oscilloscope (MSO) MSO7045B (Agilent Technologies). A single-phase FLUKE 43 B power quality analyzer is used to measure the THD and harmonic order of the output voltage. The apparatus used for the experimental study is depicted in Fig. 7.

Figure 8 shows the harmonic spectrum of output voltage obtained up to 49th order. The electronic circuit of the ND-SDCMI is depicted in Fig. 9. Figure 10 shows the 12-level output voltage of ND-SDCMI, the output voltage has 12 levels, the rms value of output voltage is 7.9 V, and the THD is 4.7%. The experimental results concur with simulation results.
Conclusion

The ND-SDCMI uses fewer components than existing topologies do to generate the same number of levels of output voltage. Maximum blocking voltage of the ND-SDCMI topology does not change with an increase in the number of levels; therefore, the overall cost of the MLI is reduced. Electronic circuit for experimental study has been designed. The efficiency of the proposed topology is greater than 92% if it is operated at duty cycles varying from 0 to 4.5 and from 0.55 to 1. Simulation results have been obtained for the load voltage, load current, THD, voltage across the inductor, and blocking voltage. Experimental results have been obtained for the output voltage, THD, voltage across the inductor and gate pulses of H-bridge. The experimental results indicated that the 12-level ND-SDCMI topology gives less than 5% THD in the output voltage. Experimental results were validated with those obtained by simulation.

References

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22 Fathabadi, H., High benefits approach for electrical energy conversion in electric vehicles from DC to PWM-AC without any generated harmonic, Energy conversion and management, 77(2014) 324-333


Nomenclature

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{in}$</td>
<td>Input DC voltage of proposed SDCMI</td>
</tr>
<tr>
<td>$N_{switch}$</td>
<td>Number of semiconductor switch</td>
</tr>
<tr>
<td>$V_L$</td>
<td>Voltage across inductor</td>
</tr>
<tr>
<td>$D$</td>
<td>Duty cycle</td>
</tr>
<tr>
<td>$i$</td>
<td>Current flowing through SDCMI</td>
</tr>
<tr>
<td>$N_{other}$</td>
<td>Other components used</td>
</tr>
<tr>
<td>$T_{ON}$</td>
<td>Turn ON time of gate signal</td>
</tr>
<tr>
<td>$T_{OFF}$</td>
<td>Turn OFF time of gate signal</td>
</tr>
<tr>
<td>$L_{inductor}$</td>
<td>Inductor</td>
</tr>
<tr>
<td>$P_{out}$</td>
<td>Output power</td>
</tr>
<tr>
<td>$V_{RL}$</td>
<td>Voltage across load</td>
</tr>
<tr>
<td>$P_{Loss}$</td>
<td>Loss in the proposed SDCMI</td>
</tr>
<tr>
<td>$V_Q$</td>
<td>Forward voltage drop of semiconductor switch</td>
</tr>
<tr>
<td>$V_{block}$</td>
<td>Maximum blocking voltage of SDCMI</td>
</tr>
<tr>
<td>$R_{ON}$</td>
<td>ON resistance of semiconductor switch</td>
</tr>
<tr>
<td>$h$</td>
<td>H-bridge</td>
</tr>
<tr>
<td>$\Delta i$</td>
<td>Ripple current</td>
</tr>
<tr>
<td>$n$</td>
<td>Number of levels in output voltage</td>
</tr>
<tr>
<td>$T$</td>
<td>Transformer</td>
</tr>
<tr>
<td>$F$</td>
<td>Frequency of output voltage of proposed SDCMI</td>
</tr>
<tr>
<td>$T_s$</td>
<td>Steady state time of buck converter output voltage</td>
</tr>
<tr>
<td>$v_f$</td>
<td>Fundamental voltage of proposed SDCMI</td>
</tr>
<tr>
<td>$T_F$</td>
<td>Time period of output voltage of proposed SDCMI</td>
</tr>
<tr>
<td>$x$</td>
<td>Harmonic order of the output voltage</td>
</tr>
<tr>
<td>$i_{RL}$</td>
<td>Load current</td>
</tr>
</tbody>
</table>