MOS capacitor integrated microstrip antenna

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An MOS capacitor integrated microstrip antenna is proposed, in which the operating frequency of the rectangular microstrip antenna is electronically controlled with the bias voltage of the MOS capacitor. Theoretical investigations based on a modal cavity model are carried out for the MOS capacitor integrated microstrip antenna. The tuning range was found to be 4.6836 GHz (110.08 %) in comparison to that (76.08 %) reported earlier.

Keywords: Microstrip antenna, MOS capacitor integrated patch antenna, Frequency agility, Stacked antenna, Patch antenna

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1 Introduction

The microstrip antenna has numerous inherent advantages, e.g. low profile, light weight, easy fabrication and suitability of mass production. There has been enormous research and development in this area. Due to compatibility with planar solid-state devices in addition to diversified applications, it has also been found suitable in satellite communications, radars, missiles, high-speed space vehicles and other strategic defence equipments. In spite of numerous advantages, the microstrip antenna has a low power handling capability, low bandwidth and poor efficiency, which limit its applicability. Active solid-state devices can be integrated with patch to improve the antenna performance. Further improvements in power and bandwidth can be achieved by stacking the antenna.

Various forms of stacked microstrip antenna with different shapes depending on different applications have been proposed with various methods of feeding mechanism involving coaxial probe, microstrip line, slot line and gap coupling. In the present work, an MOS capacitor integrated stacked microstrip antenna is analyzed to predict the radiation characteristics of the proposed radiating structure. The analysis of the two-layer electromagnetically coupled rectangular microstrip patch is based on modal expansion cavity model. The lower element is MOS capacitor integrated patch, which is coaxially fed cavity resonator, while the upper one is electromagnetically coupled cavity resonator.

The analysis carried out concentrates on the MOS capacitor integrated patch as well as MOS capacitor integrated stacked microstrip antenna with a view to comparing the performance of the two structures so far as their radiation parameters are concerned. The details of entire investigations are given in the following sections.

2 Theoretical considerations

2.1 MOS capacitor

An MOS capacitor of MIS (metal-insulator-semiconductor) diode is a voltage variable capacitor. Figure 1 shows a typical Au-Si₃N₄-Si MOS capacitor structure for the proposed analysis. The capacitance is dependent on the oxide thickness, hence

\[ C = \frac{\varepsilon A}{d} \text{ (in F)} \]  \hspace{1cm} \ldots (1)

where \( \varepsilon = \varepsilon_r \varepsilon_0 \) is the permittivity of the substrate material (F m⁻¹), \( A \) is the cross-section area of the device (m²) and \( d \) is the Si₃N₄ layer thickness (Å).

Figure 1(c) shows the equivalent circuit of the device. The capacitor \( C_0 \) is a variable capacitance known as depletion layer capacitance which is varied with bias voltage, whereas capacitance \( C_0 \) is the insulator capacitance which is fixed. The MOS capacitance per unit area can be given as

\[ C = \frac{\varepsilon A}{d} \text{ (in F)} \]
where the values of $C_D$ and $C_0$ are defined for unit area and

$$C_D = \frac{\varepsilon}{\chi}$$

is the width of the depletion layer, $\varepsilon = \varepsilon_r \varepsilon_a$ is the permittivity of the semiconductor material, $N_a$ the acceptor concentration of the doping material, $V_g$ the gate bias voltage and $q$ the charge of the electron. Combining Eqs (2) and (3), we have

$$C_{\text{mos}} = \frac{C_0}{1 + \frac{C_0}{C_D}}$$  \hspace{1cm} \ldots (2)$$

$$C_{\text{mos}} = \frac{C_0}{1 + \frac{2V_g C_0^2}{\varepsilon q N_a}}$$  \hspace{1cm} \ldots (3)$$

Evidently Eq. (4) shows that the value of MOS capacitance decreases with gate potential. The net MOS capacitance is obtained as

$$C_{\text{mos}} = \left[ \frac{C_0}{1 + \frac{2V_g C_0^2}{\varepsilon q N_a}} \right] A$$  \hspace{1cm} \ldots (4)$$

$$C_{\text{mos}} = \frac{C_0}{1 + \frac{2V_g C_0^2}{\varepsilon q N_a}}$$  \hspace{1cm} \ldots (5)$$

Fig. 1—Schematic representation of MOS capacitor and its equivalent circuit

Fig. 2—Schematic representation of MOS capacitor loaded microstrip antenna

2.2 MOS capacitor loaded rectangular microstrip antenna

Figure 2 shows a rectangular microstrip patch antenna loaded with the MOS capacitor. The diode placement location $D$ is given by

$$D = \frac{\lambda_g}{2\pi} \cos^{-1} \left[ 2Z_m G_r \left( \frac{1 - G_m}{G_r} \right) \right]^{1/2}$$  \hspace{1cm} \ldots (6)$$

where $G_t = b^2/90A_0^2$ is the radiation conductance, $G_m$ the mutual conductance of the two edges of the antenna, $G_t/G_m = 0.32$, $Z_m$ the input impedance of the antenna at the MOS capacitor location, $\lambda_g$ the guided wavelength and $(W - D, l/2)$ the MOS capacitor location (coordinate).

The equivalent circuit of a rectangular patch microstrip antenna is a parallel combination of resistance $R$, inductance $L$ and capacitor $C$. According to the modal expansion cavity model, the values of $R$, $L$ and $C$ are given as

$$C = \frac{\varepsilon_0 \varepsilon J W}{2h} \cos^{-2}(\pi y_0/l)$$  \hspace{1cm} \ldots (7)$$
where, $c$ is the velocity of light; $\omega=2\pi f_r$, $f_r$ is design frequency, $Q_t$ the radiation quality factor, $\varepsilon_e$ is the effective permittivity of the medium and given by,

$$
\varepsilon_e = \frac{\varepsilon_r + 1}{2} + \frac{\varepsilon_r - 1}{2} \left(1 + \frac{10h}{W}\right)^{\frac{1}{2}}
$$

where, $\varepsilon_r$ is the relative permittivity of the substrate material, $l$ the length of the patch, $W$ the width of the patch and $h$ the thickness of the substrate.

The total quality factor of the rectangular microstrip patch can be given as

$$
Q_T = Q_t \left(1 + 2\frac{R_1 + R_2}{R_t}\right)
$$

where,

$$
Q_t = \frac{c \sqrt{\varepsilon_e}}{4 f_r h}
$$

(radiusion quality factor)

$$
R_t = \frac{120 \pi^2}{l_1}
$$

(radiusion resistance)

where $l_1 = \frac{\pi}{2} \sin^{-1} \left(\frac{k_0 W \cos \theta}{2}\right) \tan^3 \theta \sin \theta \ d\theta$

$$
R_c = 0.00027 \sqrt{f_r \frac{l}{W}} Q_t^2
$$

(copper loss resistance),

where $f_r$ in GHz

$$
R_d = \frac{30 \tan \delta \ h \lambda_0 Q_t^2}{\varepsilon_r l W}
$$

(dielectric loss resistance)

Figure 3 shows the equivalent circuit when the patch is under excitation. The patch performance will also be affected due to its radiating edge capacitance in addition to the capacitance offered by the MOS capacitor. Under this condition, the total capacitance will be

$$
C_{\text{total}} = C_{\text{mos}} + C_s + C_d
$$

... (13)
The equivalent circuit of the electromagnetically coupled rectangular microstrip stacked antenna is shown in Fig. 5. The amount of coupling has been calculated using quality factors of the two cavity resonators. The maximum radiation will occur when both cavity resonators are in action. If $V_1$ is the voltage across the active patch and $V_2$ is the voltage across the parasitic patch, then, at the resonance, the response in the parasitic element can be written as

$$\frac{V_2}{V_1} = \sqrt{\frac{L_p}{L_d}} \left( \frac{k}{k_c^2 + \frac{1}{Q_d Q_p}} \right)$$

where:
- $L_d$ = Inductance of the active patch
- $L_p$ = Inductance of the parasitic element
- $Q_d$ = Quality factor of the active patch
- $Q_p$ = Quality factor of the parasitic element
- $k$ = Actual coefficient of coupling
- $k_c$ = Critical coefficient of coupling

The parasitic element will have maximum response when the actual coefficient of coupling equals the critical coupling (i.e., $k = k_c$). Hence

$$\frac{d}{dk} \left( \frac{k}{k_c^2 + \frac{1}{Q_d Q_p}} \right) = 0$$

or

$$\frac{1}{k_c^2} + \frac{1}{Q_d Q_p} = 0$$

or

$$k_c = \frac{1}{\sqrt{Q_d Q_p}}$$

where $k_c$ is the coupling coefficient between the patches and $Q_d$ and $Q_p$ are the total quality factor of the first and second resonator, respectively. Considering both inductive and capacitive coupling, the resulting equivalent circuit of the stacked antenna can be represented as in Fig. 5 and the values of mutual inductance $L_m$ and mutual capacitance $C_m$ are defined as

$$L_m = \frac{k_c^2 (L_d + L_p) \sqrt{k_c^2 (L_d + L_p)^2 + 4k_c^2 (1-k_c^2)L_d L_p}}{2(1-k_c^2)}$$

$$C_m = \frac{-(C_d + C_p) + \sqrt{(C_d + C_p)^2 - C_d C_p (1-1/k_c^2)}}{2}$$

The resonant frequency of the proposed structure can be obtained as

$$f_r = \frac{1}{2\pi \sqrt{L_i C_i}}$$

where

$$L_i = L_d L_p + L_m$$

$$C_i = \frac{(C_d + C_p) C_m}{C_d + C_p + C_m}$$
where $L_d, C_d$ and $L_p, C_p$ are the inductance and capacitance of the lower and upper patch, respectively.

### 2.4 Input impedance, VSWR and return loss

Using Fig. 5, input impedance of the proposed structure can be obtained as

$$Z_{in} = \frac{j\omega R_i L_i}{j\omega L_i + R_i - \omega^2 R_i L_i C_i} \quad \ldots \quad (18)$$

where $R_i = \frac{R_d R_p}{R_d + R_p}$

where $R_d$ and $R_p$ are the driven patch resistance and parasitic patch resistance, respectively. The reflection coefficient ($\rho$) can be calculated as

$$\rho = \left| \frac{Z_{in} - Z_0}{Z_{in} + Z_0} \right| \quad \ldots \quad (19)$$

where, $Z_0$ is impedance of the coaxial feed (50$\Omega$) and hence VSWR is calculated as

$$VSWR = \frac{1 + |\rho|}{1 - |\rho|} \quad \ldots \quad (20)$$

The return loss of the antenna is given by

$$RL = -10\log \frac{1}{|\rho|^2} \quad \ldots \quad (21)$$

### 2.5 Radiation pattern

The far-field radiation pattern in the $E$ plane using these equations can be obtained as

$$E_\theta = \frac{\eta_0 W \Pi_{t1} (1 + k_c) \sin \omega (t - \frac{r}{c})}{4\pi rc} \cos (k t \cos \theta)$$

$$= \left[ \sin \left( \frac{k_d l}{2} \sin \theta \sin \phi \right) \right] \left[ \cos \left( \frac{k_d W}{2} \sin \theta \cos \phi \right) \right] \cos \phi; \quad 0 \leq \theta \leq \pi / 2$$

$$E_\varphi = \frac{\eta_0 W \Pi_{t1} (1 + k_c) \sin \omega (t - \frac{r}{c})}{4\pi rc} \cos (k t \cos \theta)$$

$$= \left[ \sin \left( \frac{k_d l}{2} \sin \theta \sin \phi \right) \right] \left[ \cos \left( \frac{k_d W}{2} \sin \theta \cos \phi \right) \right] \cos \theta \sin \phi; \quad 0 \leq \theta \leq \pi / 2 \quad \ldots \quad (24)$$

where, $r$ is the distance of an arbitrary point, $k = k_d \sqrt{\varepsilon_r}, k_0 = 2\pi / \lambda, \eta_0$ is the intrinsic impedance (120$\Omega$), $W$ the width of patch and $k_c$ the coupling coefficient.

### 3 Design parameters

#### 3.1 CMOS capacitance

Typical data for the MOS capacitor used with patch are as follows:

<table>
<thead>
<tr>
<th>MOS capacitor structure</th>
<th>Au-Si$_x$N$_4$-Si $(n + 0.0005 \Omega \text{ cm})$</th>
</tr>
</thead>
<tbody>
<tr>
<td>Area (A) of cross-section</td>
<td>$1.6 \times 10^{-8} \text{ m}^2$</td>
</tr>
<tr>
<td>Thickness of oxide layers</td>
<td>100, 200, 300, 400, 500 $\text{A}$</td>
</tr>
<tr>
<td>Relative dielectric constant</td>
<td>7.5</td>
</tr>
<tr>
<td>of semiconductor ($S_i$)</td>
<td>11.9</td>
</tr>
<tr>
<td>material</td>
<td>RT-Duriod 5880</td>
</tr>
<tr>
<td>Relative dielectric constant</td>
<td>$\varepsilon_r$ material $\varepsilon_r$ material</td>
</tr>
<tr>
<td>of semiconductor ($S_i$)</td>
<td>1.45$\times 10^{-22} \text{ m}^{-3}$</td>
</tr>
<tr>
<td>Acceptor concentration ($N_a$)</td>
<td>0$-4 \text{ V}$</td>
</tr>
</tbody>
</table>

#### 3.2 Microstrip patch

Typical data for the microstrip patch are as follows:

<table>
<thead>
<tr>
<th>Substrate material used</th>
<th>RT-Duriod 5880</th>
</tr>
</thead>
<tbody>
<tr>
<td>Relative dielectric constant</td>
<td>2.2</td>
</tr>
</tbody>
</table>
Thickness of substrate material: 1.2 mm
Length \((l_1, l_2)\): 32.9 mm
Width \((W_1, W_2)\): 39.5 mm

4 Calculations

The variation of the total MOS capacitance with bias voltage for different values of oxide layer thickness \((d)\) is shown in Fig. 6. The values of resonance frequencies were calculated using Eqs (14) and (17) for MOS capacitance loaded patch and proposed structure for different values of oxide layer thickness \((d)\), respectively. The data thus obtained are shown in Fig. 7. The input impedance, VSWR and return loss were calculated using Eqs (18), (20) and (21) and the resulting data for the entire range of tunability are shown in Figs 8-10, respectively. The radiation pattern was calculated using Eq. (24) and resulting data are shown in Fig. 11.
Fig. 11—Radiation pattern for the MOS capacitor integrated microstrip antenna

5 Discussion

The value for the MOS capacitor as a function of bias voltage is shown in Fig. 6. It is observed that the variation of MOS capacitance is similar for all the five oxide thickness. It is also observed that capacitor variation is larger near zero bias, but it is small at higher bias. From Fig. 7, it is observed that the resonance frequency increases exponentially with bias voltage for different values of oxide layer thickness \(d\). It is further observed that the stacked antenna shows wide tunability (1.9129-6.5965 GHz = 4.6836 GHz) as compared to unstacked patch (1.6954-2.8867 GHz =1.1913 GHz). It is also observed that the maximum tunability is obtained for the smallest value of the oxide thickness \(d\) for both stacked and unstacked antenna. The frequency agility obtained with proposed antenna (110.08%) is much higher than that with the CMOS capacitor loaded microstrip antenna \(14\) (76.04%). Typically, the frequency agility obtained with proposed antenna is 1.45 times the value obtained with the CMOS capacitor loaded microstrip antenna. This is also corroborated from the resonance shown in the impedance plot (Fig. 8). From Figs 9 and 10, it is observed that the VSWR of the antenna remains well below 2 for the entire range of tunability and return loss is well below \(-11\) dB value for the entire range of tunability. Therefore, it is expected that the antenna performance will remain almost similar for the entire range of tunability, which is clearly indicated by the radiation pattern of the antenna as shown in Fig. 11.

References