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MOS capacitor integrated microstrip antenna

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An MOS capacitor integrated microstrip antenna is proposed, in which the operating frequency of the rectangular microstrip antenna is electronically controlled with the bias voltage of the MOS capacitor. Theoretical investigations based on a modal cavity model are carried out for the MOS capacitor integrated microstrip antenna. The tuning range was found to be 4.6836 GHz (110.08 %) in comparison to that (76.08 %) reported earlier.

Keywords: Microstrip antenna, MOS capacitor integrated patch antenna, Frequency agility, Stacked antenna, Patch antenna

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1 Introduction

The microstrip antenna has numerous inherent advantages, e.g. low profile, light weight, easy fabrication and suitability of mass production. There has been enormous research and development in this area. Due to compatibility with planar solid-state devices in addition to diversified applications, it has also been found suitable in satellite communications, radars, missiles, high-speed space vehicles and other strategic defence equipments. In spite of numerous advantages, the microstrip antenna has a low power handling capability, low bandwidth and poor efficiency, which limit its applicability. Active solid-state devices can be integrated with patch to improve the antenna performance. Further improvements in power and bandwidth can be achieved by stacking the antenna[1, 2].

Various forms of stacked microstrip antenna with different shapes depending on different applications[3-6] have been proposed with various methods of feeding mechanism involving coaxial probe, microstrip line, slot line and gap coupling[7]. In the present work, an MOS capacitor integrated stacked microstrip antenna is analyzed to predict the radiation characteristics of the proposed radiating structure. The analysis of the two-layer electromagnetically coupled rectangular microstrip patch[8] is based on modal expansion cavity model. The lower element is MOS capacitor integrated patch, which is coaxially fed cavity resonator, while the upper one is electromagnetically coupled cavity resonator.

The analysis carried out concentrates on the MOS capacitor integrated patch as well as MOS capacitor integrated stacked microstrip antenna with a view to comparing the performance of the two structures so far as their radiation parameters are concerned. The details of entire investigations are given in the following sections.

2 Theoretical considerations

2.1 MOS capacitor

An MOS capacitor of MIS (metal-insulator-semiconductor) diode is a voltage variable capacitor. Figure 1 shows a typical Au-Si_3N_4-Si MOS capacitor structure for the proposed analysis. The capacitance is dependent on the oxide thickness, hence

$$C = \frac{\varepsilon A}{d} \ (\text{in F}) \qquad \ldots (1)$$

where $\varepsilon = \varepsilon_0 \varepsilon_r$ is the permittivity of the substrate material (F m^{-1}), A is the cross-section area of the device (m^2) and d is the Si_3N_4 layer thickness (Å). Figure 1(c) shows the equivalent circuit of the device. The capacitor C_D is a variable capacitance known as depletion layer capacitance which is varied with bias voltage, whereas capacitance C_0 is the insulator capacitance which is fixed. The MOS capacitance per unit area can be given as[9, 10]

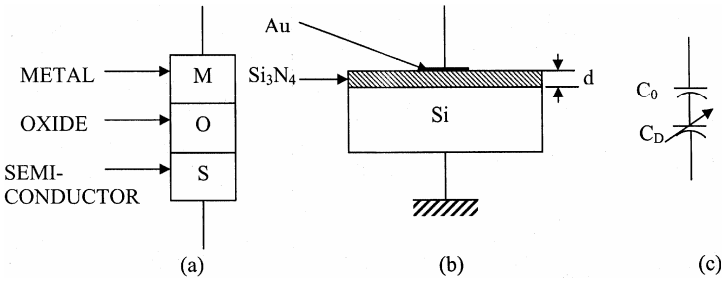

Fig. 1—Schematic representation of MOS capacitor and its equivalent circuit

$$C_{\text{mos}} = \frac{C_0}{\left(1+\frac{C_0}{C_{\text{D}}}\right)} \quad \ldots (2)$$

where the values of C_{D} and C_0 are defined for unit area and

$$C_{\text{D}} = \frac{\varepsilon}{\chi}$$

where

$$\chi = \frac{\varepsilon}{C_0}\left\{-1+\left[1+\frac{2V_{\text{g}}\,C_0^2}{\varepsilon\, q\, N_{\text{a}}}\right]^{\frac{1}{2}}\right\} \approx \frac{V_{\text{g}}}{qN_{\text{a}}} \quad \ldots (3)$$

is the width of the depletion layer, $\varepsilon = \varepsilon_0 \varepsilon_{si}$ is the permittivity of the semiconductor material, N_{a} the acceptor concentration of the doping material, V_{g} the gate bias voltage and q the charge of the electron. Combining Eqs (2) and (3), we have

$$C_{\text{mos}} = \frac{C_0}{\left[1+\frac{2V_{\text{g}}\,C_0^2}{\varepsilon q N_{\text{a}}}\right]^{\frac{1}{2}}} \quad \ldots (4)$$

Evidently Eq. (4) shows that the value of MOS capacitance decreases with gate potential. The net MOS capacitance is obtained as

$$C_{\text{mos}} = \left[\left\{\frac{C_0}{\left[1+\frac{2V_{\text{g}}\,C_0^2}{\varepsilon q N_{\text{a}}}\right]^{\frac{1}{2}}}\right\} A\right] \quad \text{(in F)} \quad \ldots (5)$$

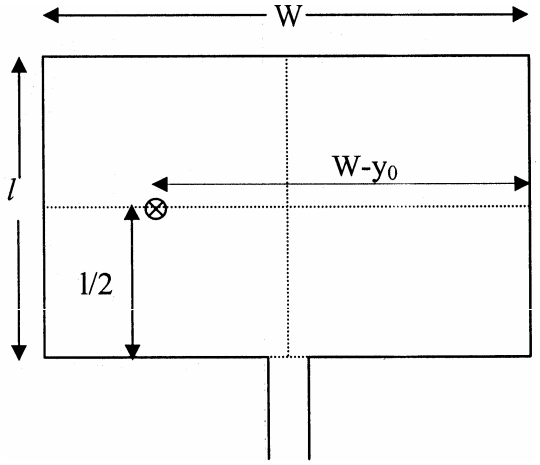

Fig. 2—Schematic representation of MOS capacitor loaded microstrip antenna

2.2 MOS capacitor loaded rectangular microstrip antenna

Figure 2 shows a rectangular microstrip patch antenna loaded with the MOS capacitor. The diode placement location D is given by[4]

$$D = \frac{\lambda_{\text{g}}}{2\pi}\cos^{-1}\left[2Z_{\text{in}}^{'}G_{\text{r}}\left(1-\frac{G_{\text{m}}}{G_{\text{r}}}\right)\right]^{l/2} \quad \ldots (6)$$

where $G_{\text{r}} = b^2/90\lambda_0^2$ is the radiation conductance, G_{m} the mutual conductance of the two edges of the antenna, $G_{\text{r}}/G_{\text{m}} = 0.32$, Z_{in} the input impedance of the antenna at the MOS capacitor location, λ_g the guided wavelength and $(W-D, l/2)$ the MOS capacitor location (coordinate).

The equivalent circuit of a rectangular patch microstrip antenna is a parallel combination of resistance R, inductance L and capacitor C. According to the modal expansion cavity model, the values of R, L and C are given as[11]

$$C = \frac{\varepsilon_0 \varepsilon_e lW}{2h}\cos^{-2}\left(\pi y_0/l\right) \quad \ldots (7)$$

$$L=\frac{1}{\omega^2 C} \quad \ldots (8)$$

$$R=\frac{Q_r}{\omega C} \quad \ldots (9)$$

$$Q_r=\frac{c\sqrt{\varepsilon_e}}{4fh} \quad \ldots (10)$$

where, c is the velocity of light; $\omega=2\pi f_r$, f_r is design frequency, Q_r the radiation quality factor, ε_e is the effective permittivity of the medium and given by[10]

$$\varepsilon_e=\frac{\varepsilon_r+1}{2}+\frac{\varepsilon_r-1}{2}\left(1+\frac{10h}{W}\right)^{-\frac{1}{2}} \quad \ldots (11)$$

where, ε_r is the relative permittivity of the substrate material, l the length of the patch, W the width of the patch and h the thickness of the substrate.

The total quality factor of the rectangular microstrip patch can be given as

$$Q_T=Q_r\left(1+2\frac{(R_d+R_c)}{R_r}\right) \quad \ldots (12)$$

where,

$$Q_r=\frac{c\sqrt{\varepsilon_e}}{4f_r h} \text{ (radiation quality factor)}$$

$$R_{r_1}=120\pi^2/I_1 \text{ (radiation resistance)}$$

where $I_1=\int_0^{\pi}\sin^2\left(\frac{k_0 W\cos\theta}{2}\right)\tan^2\theta\sin\theta\,d\theta$

$$R_c=0.00027\sqrt{f_r}\,\frac{l}{W}Q_r^2 \text{ (copper loss resistance),}$$

where f_r in GHz

$$R_d=\frac{30\tan\delta\;\; h\lambda_0}{\varepsilon_r l W}Q_r^2 \text{ (dielectric loss resistance)}$$

Figure 3 shows the equivalent circuit when the patch is under excitation. The patch performance will also be affected due to its radiating edge capacitance in addition to the capacitance offered by the MOS capacitor. Under this condition, the total capacitance will be

$$C_{total}=C_{mos}+C_s+C_d \quad \ldots (13)$$

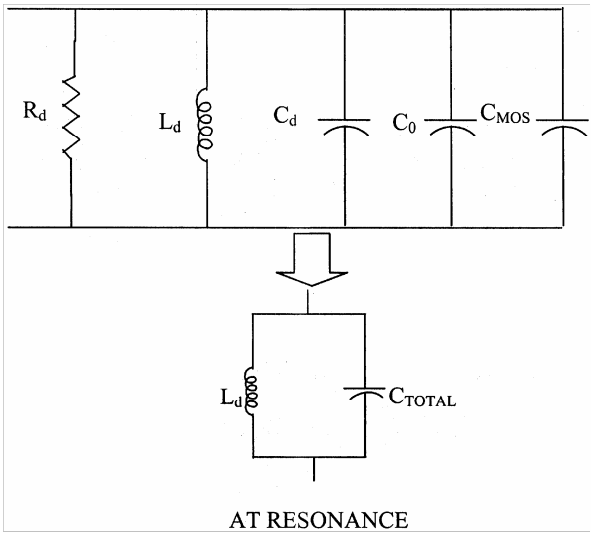

Fig. 3—Equivalent circuit of MOS capacitor loaded microstrip antenna.

where C_s is the radiating edge capacitance and given as

$$C_s=\frac{0.01668}{\omega}\left(\frac{\Delta l}{h}\right)\left(\frac{W}{\lambda}\right)\varepsilon_e \;(\text{in F})$$

where ε_e is the effective relative permittivity and Δl the fringing length. Here, it is assumed that there is no packaging R, L, C components. Thus, the resonance frequency can be given as

$$f_r=\frac{1}{2\pi\sqrt{L_d C_{total}}}$$

$$f_r=\frac{1}{2\pi\sqrt{L_d\left(C_{mos}+C_s+C_d\right)}} \quad \ldots (14)$$

2.3 Two-layer stacked patch

The configuration for an electromagnetically coupled two layer rectangular microstrip antenna with coaxial feed is shown in Fig. 4[(a)-(b)]. In the two layer patch, the lower one is the MOS capacitance integrated patch and the upper one is parasitic element. The patches are taken to be highly conductive with an effective conductivity of σ taking into account the effect of the surface roughness losses. The probe is treated to be a current element if the diameter of the probe is small. In this model, there is no air gap between the two dielectric layers which are assumed to be lossy with loss tangent, $\tan\delta$. The physical explanation is based on the cavity concept in which the lower patch is coaxial fed cavity resonator, while the

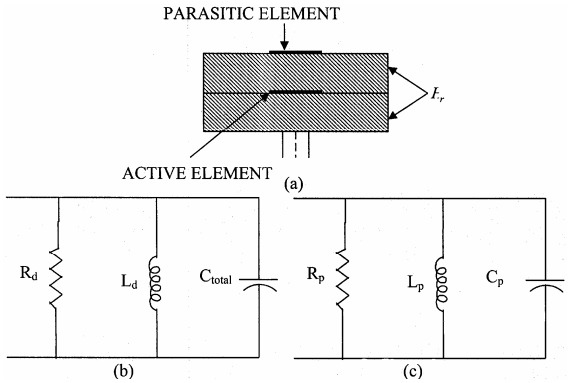

Fig. 4—(a) Side-view of two layers stacked microstrip antenna (b) Equivalent circuit of active patch (c) Equivalent circuit of parasitic patch

upper one is electromagnetically coupled cavity resonator.

The equivalent circuit of the electromagnetically coupled rectangular microstrip stacked antenna is shown in Fig. 5. The amount of coupling has been calculated using quality factors of the two cavity resonators. The maximum radiation will occur when both cavity resonators are in action. If V_1 is the voltage across the active patch and V_2 is the voltage across the parasitic patch, then, at the resonance, the response in the parasitic element can be written as[13]

$$\frac{V_2}{V_1} = \sqrt{\frac{L_p}{L_d}} \left(\frac{k}{k_c^2 + \frac{1}{Q_d Q_p}} \right) \quad \ldots (15)$$

where,

L_d = Inductance of the active patch

L_p = Inductance of the parasitic element

Q_d = Quality factor of the active patch

Q_p = Quality factor of the parasitic element

k = Actual coefficient of coupling

k_c = Critical coefficient of coupling

The parasitic element will have maximum response when the actual coefficient of coupling equals the critical coupling (i.e, $k = k_c$). Hence

$$\frac{d}{dk} \left(\frac{k}{k_c^2 + \frac{1}{Q_d Q_p}} \right) = 0$$

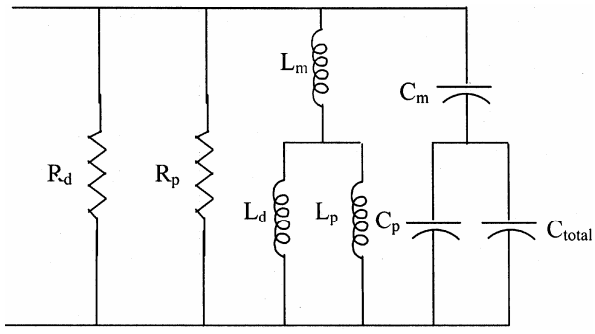

Fig. 5—Equivalent circuit of stacked microstrip antenna

$$\text{or, } \frac{1}{k_c^2 + \frac{1}{Q_d Q_p}} = 0$$

$$\text{or, } k_c = \frac{1}{\sqrt{Q_d Q_p}}$$

where k_c is the coupling coefficient between the patches and Q_d and Q_p are the total quality factor of the first and second resonator, respectively. Considering both inductive and capacitive coupling, the resulting equivalent circuit of the stacked antenna can be represented as in Fig. 5 and the values of mutual inductance L_m and mutual capacitance C_m are defined as[13]

$$L_m = \frac{k_c^2 \left(L_d + L_p\right) \sqrt{k_c^4 \left(L_d + L_p\right)^2 + 4k_c^2 \left(1 - k_c^2\right) L_d L_p}}{2\left(1 - k_c^2\right)}$$

$$C_m = \frac{-\left(C_d + C_p\right) + \sqrt{\left(C_d + C_p\right)^2 - C_d C_p \left(1 - 1/k_c^2\right)}}{2} \quad \ldots (16)$$

The resonant frequency of the proposed structure can be obtained as

$$f_r = \frac{1}{2\pi\sqrt{L_t C_t}} \quad \ldots (17)$$

where,

$$L_t = \frac{L_d L_p}{L_d + L_p} + L_m$$

$$C_t = \frac{\left(C_d + C_p\right) C_m}{C_d + C_p + C_m}$$

where L_d, C_d and L_p, C_p are the inductance and capacitance of the lower and upper patch, respectively.

2.4 Input impedance, VSWR and return loss

Using Fig. 5, input impedance of the proposed structure can be obtained as

$$Z_{in} = \frac{j\omega R_t L_t}{j\omega L_t + R_t - \omega^2 R_t L_t C_t} \quad \ldots (18)$$

where $R_t = \frac{R_d R_p}{R_d + R_p}$

where R_d and R_p are the driven patch resistance and parasitic patch resistance, respectively. The reflection coefficient (ρ) can be calculated as

$$\rho = \left| \frac{Z_{in} - Z_0}{Z_{in} + Z_0} \right| \quad \ldots (19)$$

where, Z_0 is impedance of the coaxial feed $(50\,\Omega)$ and hence *VSWR* is calculated as

$$VSWR = \frac{1 + |\rho|}{1 - |\rho|} \quad \ldots (20)$$

The return loss of the antenna is given by

$$RL = -10 \log \frac{1}{\rho^2} \quad \ldots (21)$$

2.5 Radiation pattern

The far-field radiation pattern of a rectangular patch in the TM_{10} mode[12] is broad in both the *E* and *H* planes. The expressions for *E* and *H* plane radiation pattern have been derived based on fringing field capacitance approach. Let I_{f1} be the fringing current on the driven or active patch, then the fringing current for electromagnetically coupled patch will be $k_c I_{f1}$. Thus, the total fringing current responsible for radiation is

$$I_f = I_{f1}(1 + k_c) \quad \ldots (22)$$

If the slots are considered to be symmetrical, then the current available in each slot is

$$I_{s1} = I_{s2} = \frac{I_f}{2} = \frac{I_{f1}(1 + k_c)}{2} \quad \ldots (23)$$

The far-field radiation in the *E* plane using these equations can be obtained as

$$E_\theta = \frac{\eta_0 W l I_{f1}(1 + k_c) \sin\omega\left(t - \frac{r}{c}\right)}{4\pi r c} \left[\cos(kt\cos\theta)\right] \left[\frac{\sin\left(\frac{k_0 l}{2}\sin\theta\sin\phi\right)}{\frac{k_0 l}{2}\sin\theta\sin\phi}\right] \left[\cos\left(\frac{k_0 W}{2}\sin\theta\cos\phi\right)\right]\cos\phi;$$

$$0 \le \theta \le \pi/2$$

$$E_\phi = \frac{\eta_0 W l I_{f1}(1 + k_c) \sin\omega\left(t - \frac{r}{c}\right)}{4\pi r c} \left[\cos(kt\cos\theta)\right] \left[\frac{\sin\left(\frac{k_0 l}{2}\sin\theta\sin\phi\right)}{\frac{k_0 l}{2}\sin\theta\sin\phi}\right] \left[\cos\left(\frac{k_0 W}{2}\sin\theta\cos\phi\right)\right]\cos\theta\sin\phi;$$

$$0 \le \theta \le \pi/2 \quad \ldots (24)$$

where, r is the distance of an arbitrary point, $k = k_0\sqrt{\varepsilon_r}$, $k_0 = 2\pi/\lambda$, η_0 is the intrinsic impedance $(120\pi\,\Omega)$, *W* the width of patch and k_c the coupling coefficient.

3 Design parameters

3.1 CMOS capacitance

Typical data for the MOS capacitor used with patch are as follows:

MOS capacitor structure	: Au-Si_3N_4-Si (n +0.0005 Ω cm)
Area (A) of cross-section	: 1.6×10^{-8} m^2
Thickness of oxide layers	: 100, 200, 300, 400, and 500 Å
Relative dielectric constant ε_r of (Si_3N_4) material	: 7.5
Relative dielectric constant ε_r of semiconductor (S_i) material	: 11.9
Acceptor concentration (N_a)	: 1.45×10^{22} m^{-3}
Gate bias voltage (V_g)	: $0-4$ V

3.2 Microstrip patch

Typical data for the microstrip patch are as follows:

Substrate material used	: RT-Duriod 5880
Relative dielectric constant (ε_{r1}, ε_{r2})	: 2.2

Thickness of substrate material
: 1.2 mm
Length (l_1, l_2) : 32.9 mm
Width (W_1, W_2) : 39.5 mm

4 Calculations

The variation of the total MOS capacitance with bias voltage for different values of oxide layer thickness (d) is shown in Fig. 6. The values of resonance frequencies were calculated using Eqs (14) and (17) for MOS capacitance loaded patch and proposed structure for different values of oxide layer thickness (d), respectively. The data thus obtained are shown in Fig. 7. The input impedance, VSWR and return loss were calculated using Eqs (18), (20) and (21) and the resulting data for the entire range of tunability are shown in Figs 8-10, respectively. The radiation pattern was calculated using Eq. (24) and resulting data are shown in Fig. 11.

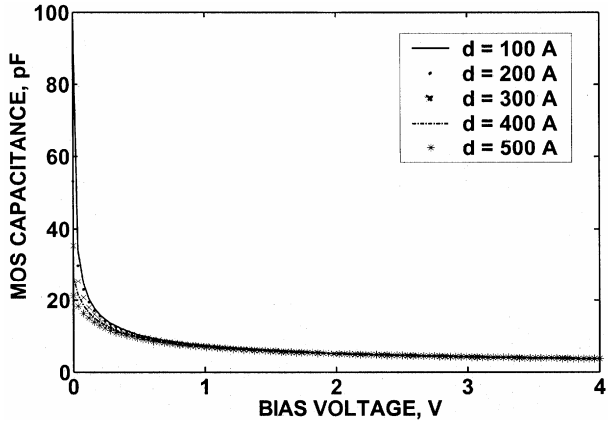

Fig. 6—Variation of MOS capacitance as a function of bias voltage

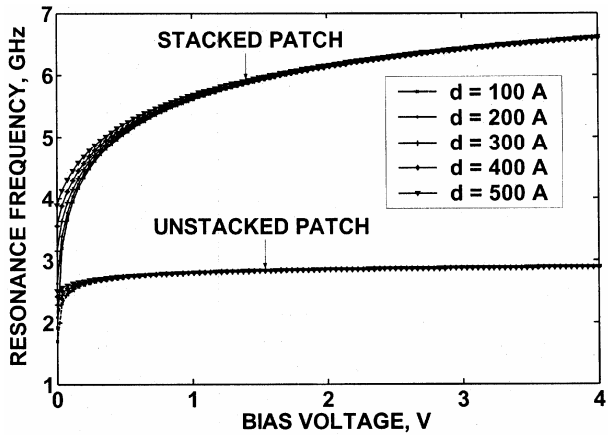

Fig. 7—Variation of resonance frequency as a function of bias voltage

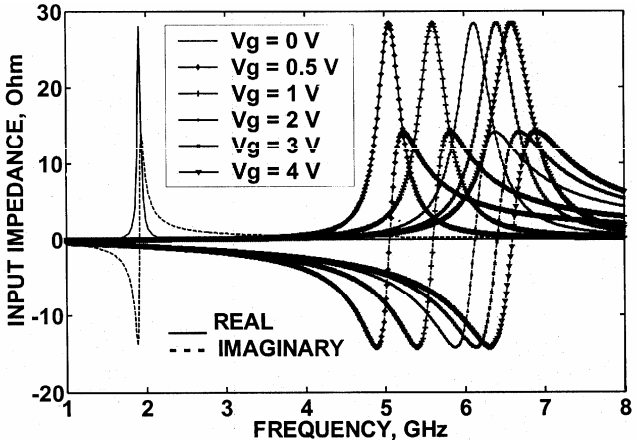

Fig. 8—Variation of impedance as a function of frequency

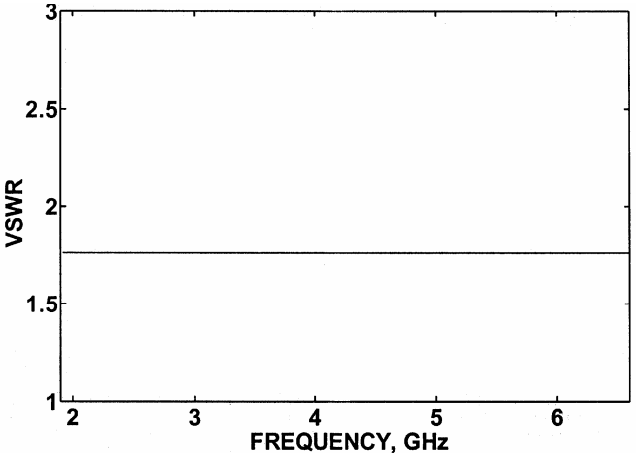

Fig. 9—Variation of VSWR as a function of bias voltage

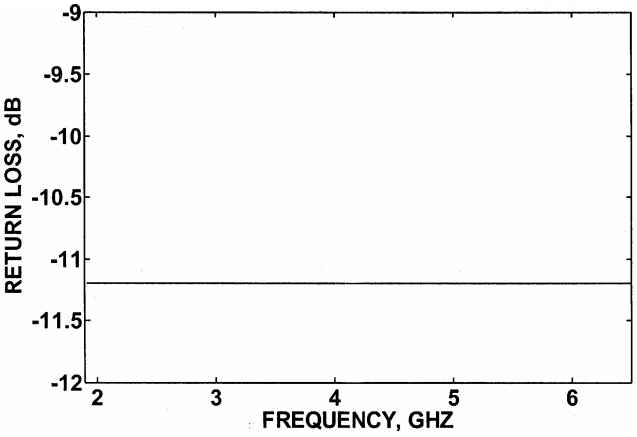

Fig. 10—Variation of return loss as a function of bias voltage

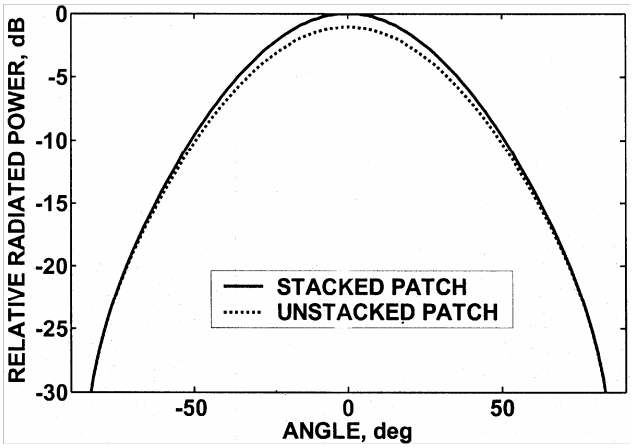

Fig. 11—Radiation pattern for the MOS capacitor integrated microstrip antenna

5 Discussion

The value for the MOS capacitor as a function of bias voltage is shown in Fig. 6. It is observed that the variation of MOS capacitance is similar for all the five oxide thickness. It is also observed that capacitor variation is larger near zero bias, but it is small at higher bias. From Fig. 7, it is observed that the resonance frequency increases exponentially with bias voltage for different values of oxide layer thickness (d). It is further observed that the stacked antenna shows wide tunability (1.9129-6.5965 GHz = 4.6836 GHz) as compared to unstacked patch (1.6954-2.8867 GHz =1.1913 GHz). It is also observed that the maximum tunability is obtained for the smallest value of the oxide thickness (d) for the both stacked and unstacked antenna. The frequency agility obtained with proposed antenna (110.08%) is much higher than that with the CMOS capacitor loaded microstrip antenna[14] (76.04%). Typically, the frequency agility obtained with proposed antenna is 1.45 times the value obtained with the CMOS capacitor loaded microstrip antenna. This is also corroborated from the resonance shown in the impedance plot (Fig. 8). From Figs 9 and 10, it is observed that the VSWR of the antenna remains well below 2 for the entire range of tunability and return loss is well below -11 dB value for the entire range of tunability. Therefore, it is expected that the antenna performance will remain almost similar for the entire range of tunability, which is clearly indicated by the radiation pattern of the antenna as shown in Fig. 11.

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