Analysis of density and time constant of interface states of MIS device by conductance method

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The density and time constant of interface states of Au/Si$_3$N$_4$/n-Si (MIS) device have been analyzed by conductance method. The capacitance and conductance measurements of the device have been performed at various frequencies in the range of 1 kHz-1 MHz. Experimental results show that $G_p/\omega$-log($f$) plots for each voltage value give a peak because of the presence of interface states. The density ($N_{ss}$) and time constant ($\tau$) of interface states have been calculated from maximum value of the peak. The values of $N_{ss}$ and $\tau$ range from $2.49 \times 10^{13}$ eV$^{-1}$cm$^{-2}$ to $7.57 \times 10^{12}$ eV$^{-1}$cm$^{-2}$ and from $2.67 \times 10^{-5}$ s to $1.67 \times 10^{-5}$ s, respectively.

Keywords: MIS device, Conductance method, Interface states, Interface state time constant

1 Introduction

The metal-insulator-semiconductor (MIS) and metal-oxide-semiconductor (MOS) devices are capacitor formed from a layer of metal, a layer of insulating or oxide and a layer of semiconductor$^1$-$^5$. The MIS and MOS devices have an insulating or oxide film thickness which is less than and more than 100 Å, respectively$^2$-$^3$. The density of interface states ($N_{ss}$) and series resistance ($R_s$) are significant parameters that cause deviation of the ideal behavior of MOS capacitor$^6$-$^9$. The interface states are located at or very close to the oxide/semiconductor interface. They cause a bias shift and frequency dispersion of capacitance/conductance-voltage (C/G-V) characteristics. Also, the interface states capacitance and resistance are associated with interface states.

In order to determine the $N_{ss}$ and $R_s$, there are various methods. Among them, the conductance method is one of the most sensitive methods proposed by Nicollian and Goetzberger$^{10,11}$. This method is based on measuring the equivalent parallel conductance of MOS device as a function of frequency and bias voltage, and it is used to extract interface states in depletion and cross-section of majority carriers. Interface states having a single trapping time constant (i.e. capture cross-section) will produce a loss peak at a frequency. Moreover, interface traps have different capture cross-section (loss peak frequency) and surface charge induced potential fluctuations produce a broadening of the loss peak$^{2,3,10-12}$.

The purpose of this study is to determine the density and time constant of interface states of Au/Si$_3$N$_4$/n-Si (MIS) device by conductance method.

2 Experimental Details

Au/Si$_3$N$_4$/n-Si (MIS) device was fabricated on phosphorus doped (n-type) single crystal Si substrate with a 2” diameter, 300 µm thickness, (100) orientation, and 0.5 Ω.cm resistivity. Before the fabrication process, the substrate was chemically cleaned using the conventional method and then chemically etched and finally quenched in deionized water. After cleaning and etching steps, the substrate was mounted on a stainless steel sputtering holder that was heated optically and loaded into a radio frequency magnetron sputtering system. The Si substrate was heated up to 400 °C in 10$^{-8}$ mbar high vacuum and sputter cleaned in pure argon ambient to ensure the removal of any residual organic substance. Then, the silicon nitride (Si$_3$N$_4$) film at a constant pressure of 3×10$^{-3}$ mbar and a constant substrate temperature of 200 °C was deposited on the substrate using high-purity (99.999%) silicon nitride target.

The ohmic and rectifier contacts were formed using a thermal evaporation system. The ohmic back contacts were formed by the deposition of high-pure Au (99.999%) with a thickness of ~2000 Å at 450 °C, under 10$^{-7}$ mbar vacuum and the sample was annealed.

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at 400 °C to achieve good ohmic contact behavior. After that, circular dot-shaped rectifier front contacts with 2 mm diameter and ~2000 Å thickness were formed by the deposition of high-purity Au onto Si$_3$N$_4$ thin film at 50 °C. The insulator layer thickness was estimated to be about 70 Å.

The C/G-V measurements were performed by using a HP 4192A LF impedance analyzer (5 Hz-13 MHz) in the frequency range of 1 kHz-1 MHz at room temperature.

3 Results and Discussion

The measured capacitance-voltage ($C_m$-V) and conductance-voltage ($G_m/\omega$-V) plots of Au/Si$_3$N$_4$/n-Si (MIS) device as a function of frequency are given in Fig. 1(a-b). As seen in Fig. 1(a-b), the value of both $C_m$ and $G_m/\omega$ decrease with increase in the frequency. The frequency dependence of the $C$ and $G/\omega$ confirms the existence of interface states in the interface of the MIS device. At the lower frequencies, the interface states follow the frequency, while at the higher frequencies they do not follow the frequency of the applied voltage. Therefore, at the sufficiently high frequencies, the contribution of interface states capacitance to the total capacitance can be neglected$^{2,3,12-19}$. Moreover, the $C_m$-V plots give a peak. The peak position shifts towards positive bias voltage with the increasing frequency. This peak can result from $R_s$ and the change of $N_{ss}$.

The $R_s$ of the MIS and MOS devices can cause a serious error in the extraction of the electrical and dielectric properties. In generally, it can be arisen from ohmic and rectifier contacts, probe wire to the gate, a dirt film or particulate matter between the back contact and the pedestal, the resistance of the quasi-neutral bulk of the semiconductor and an extremely non-uniform doping distribution in the semiconductor$^2$. The $R_s$ value of the MIS device was calculated using conductance method developed by Nicollian and Goetzberger$^{10,11}$. According to this method, the measured admittance ($Y_m$) at strong accumulation region of MIS structure using the parallel RC circuit is equivalent to the total circuit admittance as:

![Fig.1 – (a) $C_m$-V and (b) $G_m/\omega$-V plots of the MIS device as a function of frequency](image-url)
\[ Y_{\text{ma}} = G_{\text{ma}} + i\omega C_{\text{ma}} \]  \hspace{1cm} \text{...(1)}

where \( C_{\text{ma}} \) and \( G_{\text{ma}} \) are the measured capacitance and conductance in the strong accumulation region, respectively. Series resistance is the real part of the impedance \( (Z_{\text{ma}} = 1/Y_{\text{ma}}) \) and is given by the following Eq.:

\[ R_s = \frac{G_{\text{ma}}}{G_{\text{ma}}^2 + (\omega C_{\text{ma}})^2} \]  \hspace{1cm} \text{...(2)}

Figure 2 shows the \( R_s-V \) plots of the MIS device as a function of frequency. As seen in Fig. 2, the calculated \( R_s \) values decrease with increasing frequency. Such behavior of \( R_s \) is attributed to the particular distribution of localized interface states. Moreover, the \( R_s-V \) plots give a peak at about at each frequency. The magnitude of peak increases with decreasing frequency and the peak position shifts towards positive bias region (accumulation region) with decreasing frequency due to reordering and restructure of surface states under applied voltage.

\( C_m-\log f \) plots of the MIS devices, a function of forward bias voltage, are given in Fig. 3. As seen in Fig. 3, the value of capacitance decreases with the increasing forward bias voltage. After a certain value of the frequency, the measured capacitance decreases with increase in the frequency.

\( G_m/\omega-\log f \) plots of the MIS device are given in Fig. 4. As seen in Fig. 4, the value of conductance increases with the increasing forward bias voltage, while it decreases with the increasing frequency. The frequency dependence of the capacitance and conductance is attributed to the presence of a continuous distribution of interface states \(^{20-25}\).

The conductance method developed by Nicollian and Goetzberger is the most sensitive method for determining the density and time constant of interface states \(^{2,10,11}\). The conductance method is based on measuring the equivalent parallel conductance as a function of bias voltage and frequency. According to this method, the equivalent parallel conductance \( (G_p) \) can be expressed as \(^{11,26-31}\):

\[ G_p = \frac{qN_{ss}}{\omega} \ln(1 + \omega^2 \tau^2) \]  \hspace{1cm} \text{...(3)}

where \( \omega \) is the angular frequency and \( \tau \) is the time constant of the interface states (i.e. capture cross-section). In practice, different interface traps have different capture cross-section (loss peak frequency) and surface charge induced potential fluctuations produce a broadening of the loss peak. The equivalent
The values of the parallel conductance were obtained by using Eq. (4). The $G_p/\omega$ plots as a function of forward bias voltage are given in Fig. 5. As seen in Fig. 5, the $G_p/\omega$ curves for each forward bias voltage show a peak. It is clear that the peak position shifts towards higher frequencies with increase in the forward bias voltage. The magnitude of peak depends on the capture rate, that is, the interface state level occupancy that is determined by the applied bias voltage.

When the ac signal corresponds to this time constant, the loss peak associated to the interface trap levels will occur$^{21,32-37}$. Maximum loss peak occurs when interface traps are in resonance with the applied ac signal. At this peak $[\partial(G_p/\omega)/\partial(\omega\tau)=0$ and this maximum condition gives $\omega\tau=1.98$. The interface state time constant is calculated from $\tau=1.98/\omega$, where $\omega$ is the frequency at which the $G_p/\omega$ peak occurs. The $N_{ss}$ can be obtained from the parallel conductance peak using the following equation:

$$N_{ss} = \frac{(G_p/\omega)_{max}}{0.402qA} \quad \ldots(5)$$

The calculated values of the $N_{ss}$ and $\tau$ of the MIS device are given in Table 1. As seen in Table 1, the values of both $N_{ss}$ and $\tau$ decrease with increase in the forward bias voltage and are changed from $2.49\times10^{13}$ eV$^{-1}$cm$^{-2}$ to $7.57\times10^{12}$ eV$^{-1}$cm$^{-2}$ and from $2.67\times10^{-5}$ s to $1.67\times10^{-5}$ s, respectively.

### 4 Conclusions

In this study, the density and time constant of interface states of the fabricated MIS device were analyzed by capacitance-conductance-voltage measurements. The experimental results indicate that both the measured capacitance and conductance vary with applied bias voltage and frequency. The parallel conductance curves for each forward bias voltage value give a peak. The values of the $N_{ss}$ and $\tau$ calculated from the maximum value of the parallel conductance peak decrease with the increasing forward bias voltage. The obtained results indicate that the interface states affect strongly the electrical characteristics of the MIS device.

### References