Silicon drift detectors with integrated JFET: Simulation and design

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High resolution, low energy X-ray spectroscopy systems have been developed recently using the Silicon drift detector (SDD) with in-built Junction field effect transistor (JFET). A comprehensive simulation study of the SDD and integrated JFET with a view to formulate the design flow has been carried out. An optimized process flow for fabrication of SDD and integrated JFET on high resistivity detector substrate is presented. Based on these studies, several mask layouts for the SDD, JFET and reset MOSFET have been designed.

Keywords: Silicon drift detectors, MOSFET, Junction field effect transistor, X-ray spectroscopy

1 Introduction

The Silicon drift detector (SDD) is based on the principle of sideward depletion and lateral charge transport in the fully depleted bulk of the detector proposed by Gatti and Rehak\(^1\). SDD is essentially a 2-sided diode detector in which high resistivity n-type substrate is used to fabricate p-n junctions on both sides of the substrate. PN junctions on the front side are in the form of segmented strips, which act as field cathodes whereas a uniform, p-n junction forms the back-contact. Proper biasing between the anode and back p\(^+\) diode fully depletes the bulk. High voltage gradient is applied to the field shaping electrodes which creates a deep potential well that attracts free electrons produced by the passage of ionizing radiation through the detector. The surface electrodes are symmetrically connected to a voltage divider network that produces an independent electrostatic field parallel to the surface of the wafer. This field transports the signal electrons collected in the local potential well towards the anode of the detector where the charges are collected.

The most advantageous feature of SDD is small output capacitance independent of its large active area. This makes SDD best suited candidate for high resolution and high count rate X-ray spectroscopy\(^2\) for XRF analysis etc. Commercially available SDDs give energy resolution\(^3,4\) of the order of 160 eV FWHM at 5.9 keV at -20° C. These detectors also find wide spread use in high energy physics for tracking and are being used in several experiments\(^5,6\) of Large Hadron Collider at CERN.

As these detectors are used for low energy X-ray spectroscopy, it is essential to integrate the input device of the pre-amplifier with the detector so as to avoid stray capacitance and microphonism arising due to traditional bonding between them. The integration of JFET onto the detector also facilitates better matching between detector and transistor capacitances. SDD and p-n charge coupled device detectors have been fabricated with integrated junction field effect transistor onto the detector substrate by several groups. We have carried out process and device simulation studies for developing n-channel Junction field effect transistor (NJFET) on high resistivity silicon substrate. The processing steps i.e. implant scheme, diffusion temperature cycles etc. are compatible with the PIN diode detector technology\(^7\). Technological issues involved in the development of JFET on high resistivity silicon substrate and the process simulation results are presented in this paper. The device simulations have been carried out to finalize the device structure of NJFET. The schematic diagram of radial cross-section of the SDD with integrated JFET is shown in Fig. 1.

A key feature of the detector system is its reset mechanism. The integration of reset device (active feedback resistor) and feedback capacitor along with the input JFET transistor and various types of reset devices to be integrated with JFET have been studied.
by the researchers recently. Among different devices like Pentafet, Bipolar junction transistor, MOSFET (Ref. 11), the last one has proved the most suited one for implementation at Bharat Electronics Limited (BEL), Bangalore. The process and device simulation for integrating enhancement type PMOSFET with NJFET on high resistivity silicon substrate after validating the process at BEL have been studied. The process for integration of MOSFET with NJFET has been simulated drawing inputs from the recently standardized PIN fabrication process at BEL (Ref. 13). The various process cycles like oxidation, implantation, diffusion, etc were simulated using the process parameters derived from BEL. It was found that the fabrication of NJFET with MOSFET was compatible with the BEL process.

2 Process Simulations for Optimized Process Flow

The purpose of the process simulations is to design an optimal process flow within the technological constraints associated with the limited processing steps of the detector and equipment limitations of the concerned fabrication laboratory. Usually implantation at high energy (~ 500-600 keV) is required for creating deep p-well and buried channel in the detector substrate. However, no high energy implanter and no polysilicon processes are available at associated fabrication lab where PIN diode detectors with low leakage current have been produced using standard IC fabrication technology. Therefore, it is essential to design an optimal process flow with feasible values of process parameters to achieve desired device characteristics.

The technology computer aided design (TCAD) tool was first calibrated with the fabrication lab with experimental data on sheet resistance and junction depth and the results match in close proximity with only ±10% error as shown in Table 1. This practice is very important in order to ensure validity of the process simulation results in relation to real fabrication results. Process simulations have been carried out to evolve at an optimized process flow with judicious values of implant energy, dose and thermal budget for fabrication of SDD with integrated n-channel JFET on high resistivity n-type wafer (detector substrate).

<table>
<thead>
<tr>
<th>Process</th>
<th>Experimental value</th>
<th>Simulated value</th>
</tr>
</thead>
<tbody>
<tr>
<td>P1</td>
<td>228 Ω/cm²</td>
<td>229 Ω/cm²</td>
</tr>
<tr>
<td>P2</td>
<td>237 Ω/cm²</td>
<td>232 Ω/cm²</td>
</tr>
<tr>
<td>P3</td>
<td>9.65 Ω/cm²</td>
<td>9.9 Ω/cm²</td>
</tr>
<tr>
<td>P4</td>
<td>205 Ω/cm²</td>
<td>225 Ω/cm²</td>
</tr>
<tr>
<td>P5</td>
<td>211 Ω/cm²</td>
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</tr>
<tr>
<td>P6</td>
<td>4.79 μm</td>
<td>4.70 μm</td>
</tr>
<tr>
<td>P7</td>
<td>4.50 μm</td>
<td>4.55 μm</td>
</tr>
</tbody>
</table>

Fig. 1—Schematic of the SDD structure used for device simulation study. The structure is radial cross-section of the detector. It includes an on-chip JFET fabricated in a low resistivity p-well region.

Fig. 2—Silicon drain gate of JFET function of 

![Diagram](https://via.placeholder.com/150)

Figures generate steps at substrates. The do obtain cycles, drive in energy by high implant around channel (9E12 cm⁻²) production. The p-implant temperate at 2.5 μm.

![Diagram](https://via.placeholder.com/150)
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3 Device Simulations

The device simulations have been carried out for the SDD, in-built JFET and MOSFET structures. The device structures of JFET and MOSFET generated as output of the process simulator, was input for the device simulator which solves Poisson’s equation and continuity equation for a large number of mesh points in the device region. The device structure for the SDD was defined in the device simulator programme with all the doping profile inputs from the process simulations.

3.1 Silicon drift detector

Fig. 4 shows the 2D SDD structure and the input parameters used for device simulation of SDD. Suitable boundary condition and appropriate physical
models are used to simulate the device behaviour.

There are several key points to consider in the feedback cathode design:
1. The cathode is biased on a p-type region.
2. The p+ region is biased on a p-type region.
3. The cathode region is biased on a p-type region.

After selecting the appropriate bias conditions, a change in the cathode bias conditions results in a change in the device's electronic behaviour.

The simulated SDD structure is shown in Figure 5. The structure includes a chain resistor between the cathode and the horizontal current connection. During this simulation, the resistor is used to produce a current flow that is used to generate a signal.

Fig. 3—Cross-section of the device along the MOSFET structure and feedback capacitor. The structure of the device is generated after simulating each processing step in ATHENA. The p+ gate of JFET is also the drain of the integrated MOSFET.

Fig. 4—Simulated SDD structure with input parameters to the device simulator.

Implanted Resistors

- 4 kΩ-cm n-type NTD <111> 300 μm
- p+ peak concn = 1E18/cm³
- Resistor between concn = 1E15/cm³
- Anode Width = 100 μm
- p+ strip pitch = 120 (70 + 50) μm
- lx = 0.5 μm

Fig. 5—Potential variation between the horizontal cathode 1 = -100 V.
models are given as input parameters for accurate behaviour of device characteristics as in reference\(^{13}\). There are 15 electrodes in the SDD structure (8 field shaping electrodes i.e. cathodes 1-8, \(n^+\) anode and back cathode, JFET source, JFET drain, JFET gate (also MOSFET drain), MOSFET source, \(p^+\) guard ring). The used simulation tool allows defining of at most 50 regions and 20 electrodes in any device structure enough for simulation of any micro-electronic device.

After generating the structure with justified selection of grid points, the device operation and change in its characteristics by simulating different bias conditions at the electrodes were studied. Only the end cathodes (C1 and C8, back cathode) were biased on the structured side to establish sideward depletion and lateral electric field. Values of voltages applied to the electrodes were anode = 0 V, cathode 1 = -5 V, cathode 8 = -100 V, back cathode = -50 V. The detector gets fully depleted at around -20 V under the above mentioned biasing conditions. While the cathodes C1 and C8 are biased externally at -5 V and -100 V respectively, the intermediate cathodes C2 - C7 get biased automatically through the resistances between the strips.

Figure 5 shows potential distribution in the device structure at the surface and centre (150 \(\mu\)m deep). Figure 5 shows unequal potential drop across the chain resistive regions i.e. it is the highest for the resistor between C7 - C8 and lowest for the one between C1 - C2. This corresponds to the bulk current contribution in the bias resistor chain current. During this simulation, bulk properties were such as to produce huge leakage current. When the bulk generation current is reduced down to low value in the range a few nano Amperes, the non-linearity between the potential drops to negligibly small value. The horizontal potential distribution at center of the bulk is smooth and linear. The channel of the signal electrons lies deep in the bulk along diagonal of the structure. The electric field along the channel is around 800 V/cm. Corresponding to this value of field and an electron mobility of 1350 cm\(^2\)/Vs at 300 K, electron drift velocity works out to be $1.051 \times 10^6$ cm/s. This implies a detector response time (drift time) of around 100 nano seconds for a drift distance of around 1000 \(\mu\)m. Based on these simulations, one can design a SDD of circular geometry (hexagonal or square). Value of resistance between biasing electrodes is 600 k\(\Omega\) for \(W = 40 \mu\)m which corresponds to a total chain current of around 25 \(\mu\)A under the biasing conditions. The detector output capacitance at full depletion is around 93 femto Farad which is flexible enough to play with and tune it with the integrated transistor capacitance.

Fig. 6 (a and b) shows the leakage current of the detector as a function of reverse bias applied to

![Fig. 6](image-url)
cathode C8 and the CV characteristics of the proposed SDD structure respectively. As the reverse bias is increased, the depletion region extends as function of \( \sqrt{V} \) from both sides of the device. The capacitance decreases to significant low value during initial reverse bias of -5 V when the depletion region from first strip touches the n⁺ anode. Further increase in reverse bias continues to deplete the bulk (and reduce the capacitance) till full depletion is reached at -20 V. Beyond this bias, there is no decrease in capacitance which saturates to a low value corresponding to a parallel plate capacitor of area that of anode and spacing between the plates being the detector thickness.

3.2 Junction field effect transistor (JFET)

The JFET device structure generated in process simulator was exported to the device simulator and device characteristics studied. The JFET was biased in common source configuration with the source at OV and drain voltage of 15 V and gate voltage varied from 0 V to -10 V. Fig. 7 shows the \( I_D-V_{DS} \) (drain) and \( I_D-V_{GS} \) (transfer) characteristics of the JFET having gate width of 190 \( \mu \)m. The resultant pinch-off voltage is \( V_P = -5 \) V and the saturation drain current is \( I_S = 3 \) mA (Fig. 7). The transconductance at \( V_{GS} = 4 \) mA and \( V_{DS} = 15 \) V is \( g_m = 1.1 \) mS. The channel resistance in the linear region is \( \sim 1 \) kΩ. The slope of the \( I_D-V_{GS} \) curve in the saturation region corresponds to an output resistance of 7.5 MΩ. The gate leakage current is less than a few pA at operating conditions which would be significantly small as compared to leakage current of the detector (1 nA). This ensures shot noise contribution due to gate current is negligibly small as compared to the one associated with the detector leakage current. It was observed that the transistor does not breakdown even at 50 V of \( V_{DS} \). \( I_D-V_{GS} \) curve for \( V_{DS} = 0 \) V for \( V_{DS} \) up to 50 V. The gate to source capacitance at operating bias is 200 fF. The gate capacitance is in such a range that output capacitance of the SDD can be matched to get optimal results.

Fig. 7—(a) \( I_D-V_{GS} \) characteristics of NJFET with \( W = 190 \) \( \mu \)m. (b) \( I_D-V_{DS} \) characteristics of the same device.

3.3 Reset

The function of the feedback resistor to reset the thermal device is to continue the linear degradation of the detector in a known manner. A fast discharge resistor is known to conform to a fast exponential discharge steps.

The mosfet is functional in a continuous feedback resistor feedback chain. The most critical input does not contribute to the output signals from the depth information, the equivalent noise is known by the channel.

\[ ENC_{out} = \frac{i_f}{C_{eq} + C_{load}} \]

where \( i_f \) signifies the worsened in depth. Consider the simulation of the typical value capacitance of the output device.

From the saturation region, the input by the channel.
3.3 Reset MOSFET

The MOSFET was simulated with a fully functional JFET and its characteristics were extracted. Fig. 8 shows the characteristics of the simulated MOSFET. The integration of a simple resistor in the feedback loop would not be practical as large value of resistance (≈ 500 MΩ) would be required due to its thermal noise considerations. Therefore, an active device like PMOSFET should be used for the purpose. The purpose of the reset device is to provide a continuous discharge of the feedback capacitor and a dc path for the detector leakage current. Due to non-linear dependence of \( I_D \) on \( V_{GS} \), output response of the amplifier would not be exponential, but would show a faster return to zero with respect to an ideal resistive discharge of same time constant. However, it is known that output response reduces to an almost exponential function for small values of output steps.12

The main aim behind integration of JFET on the detector chip is to achieve low noise performance. The most significant aspect of JFET to be used as input device of the pre-amplifier is its noise contribution. The issues relating to processing of signals from solid state detectors have been covered in depth by Gatti and Manfredi.15 An expression for the equivalent noise charge is as follows:

\[
ENC_{opt} = \alpha \left[ \frac{4qkT}{\omega_T} \left( \frac{C_D}{C_i} \right)^{1/2} \left( \frac{C_i}{C_D} \right)^{1/2} I_C I_D \right]^{1/2}
\]

where \( I_L \) = detector leakage, \( C_D \) = detector output capacitance, \( C_i \) = input capacitance of JFET and \( \omega_T \) signifies bandwidth of the transistor and \( \alpha \) represents worsening factor arising due to actual shaper. Considering the transistor parameters obtained by the simulations and detector capacitance of ≈ 200 fF (typical for an SDD) and leakage of 1 nA (actual value can be much lower), an equivalent noise charge of the order of 30 electrons has been obtained.

From the noise point of view, a MOSFET in saturation mode would contribute noise determined by the channel thermal noise given by Eq. (2).

\[
\text{Noise}_{\text{MOSFET}} = 4kT \frac{2}{3} \frac{g_m}{W/L} = 4kT \frac{2}{3} \sqrt{2\mu_C C_{ox} W L I_D}
\]

In Eq. (2), \( I_D \) is equal to the leakage current of the detector. \( W/L \) ratio can be made small to reduce the noise but the technological considerations does not allow going beyond \( W/L = 0.5 \). Therefore, integrated MOSFET transistor cannot be used in saturation mode for reset purpose rather it is advantageous to operate the device in the triode region. The dynamic resistance of the channel in sub-threshold region is independent of \( V_{DS} \) and is given by Eq. (3).
For the simulated device, gate capacitance per unit area, $C_{ox} = 2.15 \times 10^{-3} \, \text{F/} \mu \text{m}^2$, $W = 5 \, \mu \text{m}$ and $L = 10 \, \mu \text{m}$, $V_T = 5 \, \text{V}$. The dynamic resistance of the device for $V_{GS} \leq V_T$, is in the range $1 \, \text{MO} \Omega$ to around $10 \, \text{k} \Omega$. Due to minimum linewidth of technology being $4 \, \mu \text{m}$ at BEL, $W$ cannot be reduced any further for higher values of resistance. However, it is possible to do that if the devices are fabricated at fabrication labs where minimum features can be lower than $4 \, \mu \text{m}$ i.e $< 1 \, \mu \text{m}$. Then the dynamic resistance can be in the range around $5 \, \text{M} \Omega$ to $50 \, \text{k} \Omega$. Also simulations have been carried out to see the change in the JFET characteristics when the integrated MOSFET is biased to its operational voltages. The results confirm no change in the device characteristics of JFET with MOSFET biased.

$\frac{1}{\mu_p C_{ox} \left( \frac{W}{L} \right) (V_{GS} - V_T)}$ 

(3)

4 Mask Layout

The mask layout for 4" wafer for fabrication at Bharat Electronics Limited, Bangalore is being carried out. Several SDD structures with integrated JFET have been designed. Fig. 9 shows a layout consisting of two SDD structures of active-area $9 \, \text{mm}^2$ having circular and hexagonal geometry with a die size of $5.6 \, \text{mm} \times 5.6 \, \text{mm}$. The JFET geometry is maintained circular even in the hexagonal SDD structure to maintain a high $g_m$. A composite figure of all layers of circular JFET is shown in Fig. 10.

The die size is $5.6 \, \text{mm} \times 5.6 \, \text{mm}$ for all designs. SDD structures have been designed with implanted resistors for self-biasing and also without implanted resistors and separate probing pads for each biasing strip. Gate area is $1884.51 \, \mu \text{m}^2$ and the corresponding values of $C_{GS} = 480 \, \text{fF}$ and $g_m = 1.05 \, \text{mS}$ were confirmed. JFETs for high value of $g_m$ have been designed in comb structures. The anode capacitance is around $50 \, \text{fF}$. To match with many values of the final stage.

5 Conclusions

2D-device simulations have been carried out to arrive at the final stage of a detector. Several SDD structures have been designed with integrated JFET which have high resistivity and are high-resolution devices. The design of the N-JFET capacitance leakage current has been taken care of by the design of the detector. This gives us the various optimised fabrication processes at Mumbai.

Acknowledgements

The authors would like to thank Prof.
or fabrication at alore is being with integrated shows a layout of active-area 9 geometry with a hexagonal SDD composite figure of Fig. 10. for all designs, with implanted thout implanted for each biasing corresponding 1.05 mS were $g_m$ have been e capacitance is around 50 ff. The active area of the detector is around 92 mm$^2$. The JFETs have been separately designed with many varying design parameters for an accurate matching and design of the SDD with built-in JFET in the final stage.

5 Conclusions

2D-device simulations have been carried out in order to arrive at a design for the silicon drift detector and JFET together with PMOSFET. On the basis of these studies, the mask layout for the detector and JFET which includes various designs of SDD and JFET have been completed. Technological issues associated with indigenous development of NJFET on high resistivity detector grade silicon have been resolved. The device simulation results for optimal design of JFET have been presented. Noise considerations relating to the JFET coupled with detectors have been discussed. We have also carried out systematic process and device simulations for integrating the reset MOSFET transistor within the NJFET for continuous discharge of feedback capacitance and providing $dc$ path for the detector leakage current. All the technological constraints have been taken into consideration for practical feasibility of the device fabrication. These simulation studies provide us with the preliminary design parameters for the various process parameters and these will be optimised further by experimental studies at the IC-fabrication facilities at Indian Institute of Technology, Mumbai.

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