Single voltage controlled CMOS grounded resistors and their application to video filter

Erkan Yucea, Shahram Minaeib* & Halil Alpaslan

aDepartment of Electrical and Electronics Engineering, Pamukkale University, 20070 Kinikli-Denizli, Turkey
bDepartment of Electronics and Communications Engineering, Dogus University, Acibadem, Kadikoy 34722, Istanbul, Turkey

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Two grounded voltage controlled resistors operating in saturation region are proposed. The first proposed grounded voltage controlled resistor employs 8 metal-oxide semiconductor (MOS) transistors and the second one uses 10 MOS transistors. The proposed GVCRs having only one control voltage do not need any bias currents and voltages constructed with extra elements. One of the main properties of the proposed tunable resistors is to operate at higher frequencies. The first proposed tunable resistor needs a matching condition between power supply voltages while the second does not require such a matching constraint. A video filter example for the proposed tunable resistors is also given. A number of simulations with SPICE simulation program are included in order to exhibit effectiveness, performance and workability of the proposed tunable resistors.

Keywords: Tunable resistor, MOS, Video filter, Voltage controlled

Literature survey shows that electronically controlled resistors can be replaced instead of resistive components of topologies such as analog filters and oscillator circuits. Grounded voltage controlled resistors (GVCRs) can be adjusted via control voltage(s) in metal-oxide semiconductor (MOS) process or through bias currents in MOS technology and in bipolar junction transistor (BJT) design. The GVCRs in refs1-5 operate for only positive input voltages/currents and have one or more n-channel (NMOS) transistors in triode region yielding a limited dynamic range for input signal. In addition, the circuit in ref.3 employs a current source which must be realized with additional transistors. The GVCR of refs4,5 use nine and five MOS transistors, respectively. In addition the circuits of refs4,5 do not have all MOS transistors in saturation, which yields non-linearity. The GVCRs of refs6,8 require two symmetrical control voltages which need extra elements and the circuit of ref.7 includes a translinear loop based on four BJTs and requires two matched current sources. Other interesting examples for GVCRs are found refs9-12. The circuit in ref.9 is composed of two transistors working in triode region and can realize high values of resistance (>10 MΩ) suitable for biomedical applications. In ref.10, a single voltage controlled resistor based on a voltage adder circuit employing 7 MOS transistors is presented. Also, a GVCR with a single control voltage comprising 17 transistors is reported in ref.11. However, the circuits in refs9-11 are based on ohmic (triode) operation of a transistor. In ref.12, a floating tunable resistor, independent of threshold voltage, employing 20 MOS transistors is introduced. Besides, a new grounded to floating resistor conversion topology with CMOS based two matched voltage controlled grounded resistors is described in ref.13. In ref.14, a JFET based grounded resistor is proposed. In addition, an interesting grounded resistor employing only five MOS transistors is reported in ref.15. The resistor value of the circuit in ref.15 is independent from threshold voltages. However, since four of transistors are stacked (in worst case) between power supplies (VDD and –VDD) it is not suitable for low voltage operation.

In this paper, MOS transistor based two GVCRs are proposed. The first proposed grounded voltage controlled resistor contains 8 MOS and the second one includes 10 MOS transistors. The realized GVCRs have only a single control voltage for electronic tuning of their resistive values. The introduced GVCRs do not require any extra bias currents and voltages. The first introduced GVCR
needs a matching condition between power supply voltages whereas the second one does not require any matching constraints. All of the transistors in the proposed GVCRs operate in saturation region. A video filter example is given to test the proposed GVCRs. Some analyses with SPICE simulation program are given to confirm the claimed theory.

Proposed Controlled Resistors

The equivalent circuit of a single voltage controlled GVCR is depicted in Fig. 1, which has one input port and one control voltage \( V_C \). The resistive component of GVCR is tuned electronically via control voltage and its value is defined as:

\[
Z_{in} = \frac{V}{I_{in}} = f(V_C) \quad \ldots (1)
\]

The first introduced GVCR with symmetrical power supply voltages \( V_{SS} = -V_{DD} \) is shown in Fig. 2. Assuming that all transistors are operating in saturation region, the drain currents of \( M_1 - M_4 \) transistors can be found as:

\[
I_{D1} = \frac{k_{n1}}{2} (V_{DD} - V_{TN} - V_m)^2 (1 + \lambda_n V_{DS1}) \quad \ldots (2a)
\]

\[
I_{D2} = \frac{k_{n2}}{2} (-|V_{TP}| - V_C)^2 (1 + \lambda_n V_{SD2}) \quad \ldots (2b)
\]

\[
I_{D3} = \frac{k_{p3}}{2} (V_{in} - |V_{TP}| - V_C)^2 (1 + \lambda_p V_{SD3}) \quad \ldots (2c)
\]

\[
I_{D4} = \frac{k_{n4}}{2} (V_{DD} - V_{TN})^2 (1 + \lambda_n V_{DS4}) \quad \ldots (2d)
\]

Here, the parameters, \( k_p \) and \( k_n \), are respectively called as transconductance parameter of the PMOS and NMOS transistors, which can be defined as:

\[
k_p = \left( \frac{W}{L} \right) \frac{k'_p}{k_p} \quad \ldots (3a)
\]

\[
k_n = \left( \frac{W}{L} \right) \frac{k'_n}{k_n} \quad \ldots (3b)
\]

In Eqs (3a) and (3b), \( k'_p = \mu_p C_o \) and \( k'_n = \mu_n C_o \) where \( \mu_p \) and \( \mu_n \) are respectively surface mobilities of PMOS and NMOS transistors, \( C_o \) is called gate capacitance per unit area. Additionally, \( W/L \) is the aspect ratio of the MOS transistors and \( \lambda \) in Eqs (2a)-(2d) is called as channel length modulation parameter ideally equal to zero \(^{16}\).

The threshold voltages \( V_{TN} \) and \( V_{TP} \) are respectively expressed as:

\[
V_{TN} = V_{TN0} + \gamma_n \left( \sqrt{2 \phi_F} + V_{SB} - \sqrt{2 \phi_F} \right) \quad \ldots (4a)
\]

\[
V_{TP} = V_{TP0} - \gamma_p \left( \sqrt{2 \phi_F} + V_{BS} - \sqrt{2 \phi_F} \right) \quad \ldots (4b)
\]

where \( 2 \phi_F \) is surface to bulk potential, \( V_{T0} \) is the threshold voltage under no body effect and \( \gamma \) is...
body-effect coefficient. In the proposed circuit of Fig. 2, \( V_{DS1} = V_{DD} - V_1 \), \( V_{SD2} = -V_{G1} \), \( V_{SD3} = V_{P} - V_{SS} \) and \( V_{DS4} = V_{P} - V_{SS} \). Note that \( M_3-M_6 \) and \( M_7-M_8 \) are operated as current mirrors.

For transistor \( M_3 \) and \( M_1 \) to be turned on we should have \( V_{in} - V_C \geq |V_{TP}| \) and \( V_{DD} - V_{in} \geq V_{TN} \), respectively. In addition to maintain the transistor \( M_4 \) in saturation region it is required that \( V_{in} \geq -V_{TN} \). Thus, the amplitude of the input signal should satisfy the following constraint:

\[
\text{Max} \{ V_C + |V_{TP}|, -V_{TN} \} \leq V_{in} \leq V_{DD} - V_{TN} \quad \ldots (5)
\]

On the other hand, for turning on the transistor \( M_2 \) and saturation operation of the transistor \( M_3 \) we should have \( V_C \leq -|V_{TP}| \) and \( V_C \geq V_{SS} + |V_{TP}| \), respectively. Thus the control voltage of the proposed MOS resistor should satisfy the following constraint:

\[
V_{SS} - |V_{TP}| \leq V_C \leq -|V_{TP}| \quad \ldots (6)
\]

Finally, input current of the proposed GVCR, \( I_{in} \), is obtained as:

\[
I_{in} = -I_{D1} - I_{D2} + I_{D3} + I_{D4} \quad \ldots (7)
\]

Selecting \( k_m = k_p = k \) \((i = 1, 4 \text{ and } j = 2, 3)\) and \( \lambda = 0 \) for all transistors, using the Eqs (2) and (7) the input resistance of the proposed GVCR is found as

\[
R_{eq} = \frac{V_{in}}{I_{in}} = \frac{1}{k(V_{DD} - |V_{TP}| - V_{TN} - V_C)} \quad \ldots (8)
\]

Note that \( R_{eq} \) in Eq. (8) has a pole \( (\omega_c) \) at high frequencies due to parasitic capacitances of MOS transistors. As a result, the impedance due to pole in frequency domain can be expressed as

\[
Z_{eq}(\omega) = \frac{V_{in}}{I_{in}} = \frac{1}{k(V_{DD} - |V_{TP}| - V_{TN} - V_C)} \cdot \frac{1}{1 + j\omega/\omega_c} \quad \ldots (9)
\]

The corner frequency in Eq. (9) can be found from the parasitic capacitive and resistive elements in the input node of the circuit as \( \omega_c = 1/(R_{eq}C) \), where \( R_{eq} = [(1/g_{mi})(1/g_{m5})] \) and \( C = C_{g1} + C_{gs} \). Here \( g_{mi} \) and \( C_{gs} \) are respectively the transconductance and parasitic capacitance appears between gate and source of the \( i^{th} \) transistor, respectively. The other parasitic capacitances/resistances are ignored for simplicity.

The second introduced GVCR is shown in Fig. 3. Assuming that all transistors are working in saturation region, the drain currents \( I_{D1}, I_{D6}, I_{D7} \) and \( I_{D10} \) can be found as:

\[
I_{D1} = \frac{k_m}{2} (V_C - V_{TN} - V_{in})^2 \quad \ldots (10a)
\]

\[
I_{D6} = \frac{k_p}{2} (V_C - V_{TN})^2 \quad \ldots (10b)
\]

\[
I_{D7} = \frac{k_m}{2} (V_{SS} - V_{TN})^2 \quad \ldots (10c)
\]

\[
I_{D10} = \frac{k_{n10}}{2} (-V_{SS} - V_{TN})^2 \quad \ldots (10d)
\]

In order to turn on the transistors \( M_1 \) and \( M_2 \) in the circuit of Fig. 3, the amplitude of the input signal should satisfy the following constraints:

\[
V_{SS} + V_{TN} \leq V_{in} \leq V_C - V_{TN} \quad \ldots (11)
\]

Like-wise, in order to turn on the transistor \( M_8 \) and keep the transistor \( M_1 \) in saturation the control voltage of the proposed MOS resistor should satisfy the following constraints:

\[
V_{TN} \leq V_C \leq V_{DD} + V_{TN} \quad \ldots (12)
\]

Finally, considering that \( I_{D8} = I_{D6} \) and \( I_{D5} = I_{D10} \), the input current of the second proposed GVCR, \( I_{in} \), is obtained as:

\[
I_{in} = -I_{D1} + I_{D6} + I_{D7} - I_{D10} \quad \ldots (13)
\]

Selecting \( k_{nl} = k \) \((i = 1, 6, 7 \text{ and } 10)\) for all transistors, using Eqs (10) and (13) the input resistance of the second proposed GVCR is found as

![Fig. 3—The second proposed GVCR](image-url)
Thus, the value of the electronic resistor can be controlled easily by changing the single control voltage $V_C$ without requiring symmetrical control or supply voltages.

Similar to the first proposed GVCR, the corner frequency of the second proposed resistor can be given as

$$\omega_C = \frac{1}{R_t C_t}$$

where

$$R_t \approx \frac{\left| g_{m1} \right|}{\left| g_{m7} \right|}$$

and

$$C_t \approx C_{gs1} + C_{gs7}.$$ 

A comparison of the proposed GVCRs with previously published ones is summarized in Table 1. It can be seen that the proposed circuits provide a single voltage control without employing transistors in triode region. Note that to prevent body effect in $M_1$, $M_2$, $M_3$ in the first proposed circuit, and $M_1$, $M_6$ in the second one they must be realized in individual wells connected to the relevant source terminal.

### Simulation Results

In this section, simulation results of the proposed GVCRs in Figs 2 and 3 are presented. All the bulk terminals of the MOS transistors used in GVCRs of Figs 2 and 3 are connected to their corresponding sources. The aspect ratios of the MOS transistors used in the simulation of the first proposed GVCR are given in Table 2. Also, control voltage, $V_C$ in Fig. 2, is chosen as $-0.5$ V resulting in $R_{eq} \approx 651 \Omega$. The total harmonic distortion (THD) variations with respect to peak of the sinusoidal input currents between 2.5 $\mu$A and 1.5 mA at 100 MHz are presented in Fig. 4 where THD is large at large signal values due to the non-linearity of the circuit. The total power dissipation and equivalent resistance of the first proposed GVCR in Fig. 2 versus

![Graph showing total harmonic distortion variations.](image-url)
control voltage, $V_C$, is tabulated in Fig. 5. It is important to note that the first proposed GVCR can be operated well for the control voltages from $V_C = -0.25\text{V}$ ($R_{eq} \approx 847\Omega$) to $V_C = -0.55\text{V}$ ($R_{eq} \approx 626\Omega$). Also, the resistor and -3dB frequency values of the GVCR in Fig. 2 can be changed by increasing aspect ratios of the NMOS transistors by $m$ times ($m \geq 1$) as illustrated in Fig. 6.

The current-voltage characteristic of the GVCR in Fig. 2 is given in Fig. 7. In order to demonstrate time-domain performance of the first proposed resistor in Fig. 2, a sinusoidal input with 0.5 mA peak current at 100 MHz is applied. The input current and the corresponding input voltage are indicated in Fig. 8. Similarly, to show the frequency-domain performance of the first proposed resistor circuit, magnitude and phase responses of the obtained resistance are given in Fig. 9. It is observed from Fig. 9 that -3dB frequency is changed between 1.57 GHz and 1.75 GHz.

The aspect ratios of the MOS transistors used in the simulation of the second proposed GVCR in Fig. 3 are given in Table 3. Also, control voltage, $V_C$, is chosen as $0.36\text{V}$ resulting in $R_{eq} = 535\Omega$. The THD variations versus peak of sinusoidal input currents at 500 MHz are presented in Fig. 10 in which THD is large at large signal values due to the non-linearity of the circuit. The total power dissipation and equivalent resistor values of the second proposed GVCR with respect to control voltage, $V_C$, are shown in Fig. 11. It is important to note that the second proposed GVCR can be operated well for the control voltages from $V_C = 0.06\text{V}$ ($R_{eq} \approx 800\Omega$) to $V_C = 0.36\text{V}$. Also, different resistor and -3dB frequency values for the GVCR of Fig. 3 can be obtained by increasing aspect ratios of the NMOS transistors by $m$ times ($m \geq 1$) as shown in Fig. 12.

Input voltage against the input current for the second GVCR is shown in Fig. 13. In order to show
time-domain performance of the second proposed resistor, a sinusoidal input current with 0.25 mA peak value at 500 MHz is applied. The input current and the corresponding input voltage are shown in Fig. 14. To demonstrate the frequency-domain performance of the second proposed resistor, magnitude and phase responses of the obtained resistance are shown in Fig. 15. The −3dB frequency is changed between 1.85 GHz and 2.57 GHz.

**Application to Video Filter**

As an application, a video filter depicted in Fig. 16 is given to test the proposed GVCRs. The filter in Fig. 16 has the following transfer function:

$$H(f) = \frac{1}{1 + j \frac{f}{f_{3dB}}}$$

### Table 3—Dimensions of MOS transistors of the second proposed GVCR in Fig. 3

<table>
<thead>
<tr>
<th>PMOS Transistors</th>
<th>W(µm)/L(µm)</th>
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<tbody>
<tr>
<td>M2 and M3</td>
<td>12.48/1.3</td>
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<tr>
<td>M4 and M5</td>
<td>58.5/1.3</td>
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<table>
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<tr>
<th>NMOS Transistors</th>
<th>W(µm)/L(µm)</th>
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<tbody>
<tr>
<td>M1, M6, M7 and M10</td>
<td>8.32/1.3</td>
</tr>
<tr>
<td>M8 and M9</td>
<td>1.3/1.3</td>
</tr>
</tbody>
</table>
\[ H(s) = \frac{s^2 + \omega_{o1}^2}{s^2 + \omega_{o2}^2} \times \frac{s^2 + \omega_{o3}^2}{s^2 + \omega_{o4}^2} \] \quad \ldots \quad (15)

Here, quality factors \( Q_1 = \omega_{o1} R_1 C_1 \), \( Q_2 = \omega_{o2} R_2 C_2 \) and resonance frequencies \( \omega_{o1} = 1/\sqrt{(L_1 C_1)} \), \( \omega_{o2} = 1/\sqrt{(L_2 C_2)} \) are obtained. If \( f_{o1} = 100 \text{ MHz}, f_{o2} = 80 \text{ MHz}, Q_1 = 3.9, Q_2 = 0.78 \), \( C_1 = 10 \text{ pF}, C_2 = 2.5 \text{ pF} \) and \( R_1 = R_2 = 621.5 \text{ } \Omega \) are chosen for the video filter in Fig. 10, \( L_1 = 0.253 \text{ } \mu\text{H} \) are found.

It should be mentioned that one can use active realizations for the floating inductor simulators instead of passive inductors of Fig. 16.

Using above values, the gain and phase responses of the video filter example in Fig. 16 are shown in Fig. 17 where ideal resistors and proposed first controllable resistors in Fig. 2 are employed. Aspect ratios \( (W/L) \) of all the NMOS transistors are changed from 5 to 7.5 by 1.25 increments. Therefore, the gain and phase responses results of the video filter with respect to frequency are shown in Fig. 18. Similarly, after 50 runs, Monte Carlo simulations of the video filter with 5% Gaussian changes of \( C_1 = 10 \text{ pF} \) and \( C_2 = 2.5 \text{ pF} \) are accomplished. Thus, the results for the gain and phase responses with respect to frequency are depicted in Fig. 19. Also, 20% Gaussian changes of the SPICE parameter \( U_0 \) (carrier mobility) are achieved. Hence, the results for the gain and phase responses with respect to frequency are depicted in Fig. 19.
Fig. 20. The output and equivalent input noise variations versus frequency by using SPICE simulation program are demonstrated in Fig. 21.

It is observed from Figs. 4-15, 17-21 that simulation and theoretical results are in good agreement as desired. However, the difference between them basically arises from the non-idealities of the MOS transistors.

Conclusions
Two grounded voltage controlled MOS resistors are proposed. The proposed controlled resistors can be replaced instead of resistive components of topologies such as analog filters, inductor simulators and oscillators to control electronically their parameters for example resonance frequency of the analog filters. The proposed GVCRs have a single control voltage for electronic tuning of their resistive values. One of the major features of the proposed tunable resistors is to work at high frequencies. The first proposed GVCR needs a matching condition between power supply voltages while it includes 8 MOS transistor. The second proposed one does not require a matching constraint between power supply voltages whereas it consists of 10 MOS transistors. Simulation results included in this paper verify the claimed theory well as expected.

References
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<th>Reference</th>
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