Study of the interface of ZnSe/GaAs(110) heterostructures

G N Chaudhari*, S V Manorana* & V J Rao

*Department of Chemistry, Shri Shivaji Science College, Amravati 444 603, India
*Physical and Inorganic Chemistry Division, Indian Institute of Chemical Technology, Hyderabad 500 007, India

Received 19 February 1996; accepted 16 July 1996

The different phases formed at the ZnSe/GaAs interface and Schottky barrier height have been studied by low angle X-ray diffraction, current-voltage and capacitance-voltage characteristics. It has been shown that three phases namely Ga2Se3, As2Se3 and Zn3As2 are formed after annealing the ZnSe films on GaAs at different temperatures. The diode characteristics improved significantly and the barrier height is found to increase with increasing annealing temperature.

ZnSe has great potential for use in blue-emitting devices because of its direct energy gap of 2.67 eV at room temperature. For the last several years there have been many attempts to succeed as well as to grow good quality heterojunction devices such as ZnSe/GaAs for light emitting devices or other similar applications. Because of its high quality and nearly lattice matching (0.25% mismatch) with GaAs1-8, ZnSe has been used to reduce the defect density at the interface. The ZnSe films have been grown by several techniques such as chemical vapour deposition9, liquid phase epitaxy10, molecular beam epitaxy11, metal organic chemical vapour deposition12 and metal organic molecular beam epitaxy13.

The present work deals with the growth of ZnSe thin films on GaAs by a simple deposition technique of liquid gas interface reaction (LGIR) technique. The interfaces are characterised by X-ray diffraction (XRD) and transmission electron microscopy (TEM). In addition, ZnSe/GaAs heterojunction diodes were fabricated and studied by current-voltage (I-V) and capacitance-voltage (C-V) characteristics.

Experimental procedure—The thin films of ZnSe were grown by a simple technique which is based on a double decomposition reaction. The reactants are an aqueous solution of zinc salts, e.g., zinc acetate and H2Se which is generated in situ by the reaction of a metallic selenide like CdSe with concentrated hydrochloric acid. The reaction is as follows:

\[
\text{CdSe} + 2 \text{HCl} \rightarrow \text{H}_2\text{Se} + \text{CdCl}_2 \quad \ldots (1)
\]

\[
\text{Zn} \left(\text{CH}_3\text{COOH}\right)_2 + \text{H}_2\text{Se} \rightarrow \text{ZnSe (film)} + 2 \text{CH}_3\text{COOH} \quad \ldots (2)
\]

The H2Se gas generated in reaction 1 reacts with zinc acetate solution and forms a thin film of ZnSe at the surface of zinc acetate solution. The reaction is allowed to take place for 2 min. The experimental set up used for ZnSe films is shown in Fig. 1. The ZnSe films are then picked up with the help of an inverted watch glass and allowed to float on deionized water in order to remove any residual reactants like zinc acetate or other soluble contaminating impurities. The films are then placed onto any desired substrates.

The n-type GaAs (110) substrates were first cleaned and degressed in boiling trichloroethylene and etched in a solution of 4:1:1::H2SO4:H2O2:H2O followed by a thorough rinse in deionized water. Just after etching the ZnSe thin films were lifted onto the GaAs substrates at 2, 35 and 90°C bath temperature and annealed at 100, 150 and 200°C in an argon atmosphere for 5 min each. For making Schottky contacts, aluminium was evaporated on GaAs through a metal mask with circular openings of 0.05 cm diameter by thermal evaporation method. The ohmic contacts were made by successively depositing Ni-Ge-Au on the back side of substrates and sintering at 440°C for 5 min in an argon atmosphere.

Results and discussion—The X-ray study was performed on a Rigaku (Model: Rotoflex RU

Fig. 1—The experimental set-up for ZnSe thin film.
Table 1—d values of polycrystalline ZnSe films from TEM data

<table>
<thead>
<tr>
<th>Ring of radius, cm</th>
<th>d values, Å</th>
<th>hkl</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Cal.</td>
<td>Lit.</td>
</tr>
<tr>
<td>0.57</td>
<td>3.2772</td>
<td>3.2730</td>
</tr>
<tr>
<td>0.93</td>
<td>2.0063</td>
<td>2.0030</td>
</tr>
<tr>
<td>1.15</td>
<td>1.6382</td>
<td>1.6350</td>
</tr>
<tr>
<td>1.45</td>
<td>1.3023</td>
<td>1.2990</td>
</tr>
<tr>
<td>1.60</td>
<td>1.1775</td>
<td>1.1561</td>
</tr>
</tbody>
</table>

2008) with a wavelength of 1.54 Å and at a grazing angle of 0.2°. XRD and TEM studies showed that the films grown at room temperature were totally amorphous. However, in case of the films grown at a higher temperature of about 90°C the corresponding electron diffraction pattern became sharper and well defined. Gold was used as the reference to calculate the camera constant of the microscope. Table 1 gives the observed d values and the literature value for cubic polycrystalline ZnSe films lifted on a copper grid at 90°C. Figs 2 a, b and c shows the electron diffraction pattern of ZnSe with bath temperature maintained at 2, 35 and 90°C respectively. It shows that the films grown at 90°C bath temperature are polycrystalline in nature. Fig. 3a gives the low angle XRD
pattern taken at a glancing angle of 2° of the ZnSe films deposited on n-GaAs (110) at 90°C bath temperature and annealed at 100°C. It is observed that at room temperature there is no inter-diffusion of any of the species of ZnSe and GaAs, whereas the 100°C annealed ZnSe/GaAs interface shows the formation of Ga₂Se₃ phase. Similar results are also reported for the formation of Ga₂Se₃ at the ZnSe and GaAs interface. Fig. 3b shows the low angle XRD pattern of the same GaAs/ZnSe system but annealed at 200°C. In this case the Ga-As bond at the interface is broken by charge transfer mechanism and two additional phases As₂Se₃, Zn₃As₂ are formed, along with trace amounts of Ga₂O₃ and As₂O₃. The oxides are expected because of the method of growth adopted.

I-V measurements were taken first on GaAs samples without ZnSe layer and then on GaAs with ZnSe overlayer for as deposited and also for those annealed 100, 150 and 200°C in an argon atmosphere for 5 min.

The value of barrier height (φₜ) determined from the I-V measurements are plotted as a function of the annealing temperature in Fig. 4. The barrier height for the Al/GaAs diodes without ZnSe layer were calculated and found to be around 0.66 eV. The barrier height is found to increase with annealing temperature. The saturation current as well as the ideality factor decreased on annealing. Furthermore, the reverse bias I-V characteristics were fairly good with very negligible leakage current.

The barrier height as determined by the C-V measurements also show the same trend as that deduced from the forward I-V curves. It is observed that the barrier height obtained from the C-V curve is higher than that estimated from the I-V characteristics. The increase of the barrier height with annealing temperature can be explained by the fact that on annealing the GaAs/ZnSe heterostructure Ga₂Se₃, As₂Se₃ and Zn₃As₂ species are formed at the interface, along with the Ga₂O₃ and As₂O₃ oxides which are responsible for the increase in φₜ.

The ideality factor (η) determined from the I-V curves is plotted as a function of the annealing temperature (Fig. 5). The η value for the GaAs without ZnSe overlayer was about 1.8 which does not represent a very good I-V characteristic. This poor ideality factor can be interpreted in various ways. Among them, the effect of tunnelling can be excluded because of the low carrier density of the substrates. The contribution due to the generation recombination current can also be eliminated since there was no deterioration of the saturation behaviour as observed with reverse bias voltage.

References