Fully differential first-order allpass filters using a DDCC

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Received 28 May 2013; accepted 13 March 2014

Two voltage-mode high input impedance differential input-differential output first-order allpass filters based on differential difference current conveyor (DDCC) are presented. Each of the proposed circuit uses one plus-type DDCC, one grounded capacitor and three resistors. The proposed circuits enjoy the features of high input impedance, tunable of the allpass gains and using only grounded capacitors. The tracking error and sensitivity analysis of the proposed circuits are given. Simulation results confirm the theoretical analysis.

Keywords: Fully differential filter, Current conveyor, Active filter, Allpass

The design of fully differential filters attracts many researchers’ attention. Fully differential circuits have the advantages of immunity from common mode noise signals, enhanced dynamic range and lower harmonic distortion. Therefore, several voltage-mode fully differential biquadratic filters were proposed.

First-order allpass filters are widely used in analog signal processing in order to transmit signals at frequencies equally well and change only the phase. Ibrahim et al. proposed a fully differential first-order allpass filter using one differential voltage current conveyor (DVCC), one resistor, one grounded capacitors and two floating capacitors. Minaei et al. proposed a fully differential first-order allpass filter using two second-generation current conveyors (CCIs), three resistors and one floating capacitor. Acosta et al. proposed a fully differential first-order allpass filter using two operational transconductance amplifiers (OTAs), one fully differential operational amplifier and four floating capacitors.

The differential difference current conveyor (DDCC) has the advantages of three high-input voltage terminals (y terminals) and arithmetic operation capability. The applications in the realization of various active filter functions using DDCCs have received considerable attention. In this paper, a new fully differential first-order allpass filter by using one DDCC, three resistors and one grounded capacitor is presented. The proposed circuit uses less active elements with respect to the previous fully differential first-order allpass filters. The proposed circuits use only grounded capacitors that are more attractive for integrated circuit implementation with respect to previous circuits.

Proposed Circuits

Using standard notation, the port relations of an ideal DDCC can be characterized by

\[
\begin{bmatrix}
V_x \\
i_{y1} \\
i_{y2} \\
i_{y3} \\
i_x
\end{bmatrix} = \begin{bmatrix}
1 & -1 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & V_{y1} \\
0 & 0 & 0 & 0 & V_{y2} \\
0 & 0 & 0 & 0 & V_{y3} \\
0 & 0 & 0 & \pm 1 & i_x
\end{bmatrix} \ldots (1)
\]

where the plus and minus signs indicate whether the conveyor is configured as a non-inverting or inverting type circuit, termed DDCC+ or DDCC-.

The proposed fully differential first-order allpass filters are shown in Fig. 1. Assume that \(V_{id} = V_{i1} - V_{i2} \), \(V_{ic} = (V_{i1} + V_{i2})/2 \) and \(V_{od} = V_{o1} - V_{o2} \), where \(V_{id}, V_{ic} \) and \(V_{od} \) denote differential-mode input, common-mode input and differential-output voltages, respectively. The output voltage of Fig. 1(a) can be expressed as:
\[ V_{od} = \frac{-sCR_2 R_3 + R_3 - R_2}{R_1(sCR_3 + 1)} V_{id} \]  \hspace{1cm} \text{(2)}

If the output \( V_{od} \) is expressed in terms of \( V_{id} \) and \( V_{ic} \) as

\[ V_{od} = A_{dm} V_{id} + A_{cm} V_{ic} \]  \hspace{1cm} \text{(3)}

then,

\[ A_{dm} = \frac{-sCR_2 R_3 + R_3 - R_2}{R_1(sCR_3 + 1)} \] and \( A_{cm} = 0 \)  \hspace{1cm} \text{(4)}

Selecting \( R_2 = 0.5R_3 \) the differential transfer function reduces to

\[ V_{od} = \frac{R_3(-sCR_3 + 1)}{2R_1(sCR_3 + 1)} \]  \hspace{1cm} \text{(5)}

The output voltage of Fig. 1(b) can be expressed as:

\[ V_{od} = \frac{sCR_2 R_3 - R_2 + R_1}{R_1(sCR_2 + 1)} V_{id} \]  \hspace{1cm} \text{(6)}

then,

\[ A_{dm} = \frac{sCR_2 R_3 - R_2 + R_3}{R_1(sCR_2 + 1)} \] and \( A_{cm} = 0 \)  \hspace{1cm} \text{(7)}

Selecting \( R_3 = 0.5R_2 \) the differential transfer function reduces to

\[ V_{od} = \frac{R_3(sCR_2 - 1)}{2R_1(sCR_2 + 1)} \]  \hspace{1cm} \text{(8)}

The gains of these two allpass filters are \( \frac{R_3}{2R_1} \) for Fig. 1(a) and \( \frac{R_2}{2R_1} \) for Fig. 1(b).

From Eqs (5) and (8) it can be seen that two fully differential first-order allpass filters are obtained at Fig. 1. Because the input terminals of the proposed first-order allpass filters are connected directly to the \( y \) terminals of the DDCC, the input terminals have the advantage of high input impedance. From Eqs (5) and (8) it can be seen that the allpass gains of the proposed circuits can be tuned by the resistor \( R_1 \). Note that, the proposed circuits require passive components matching conditions in the realizations of first-order allpass filters. Since the output impedances of the proposed circuits are not small, voltage buffers are needed while cascaded the proposed circuits to the next stages.

**Non-ideality Analysis**

Taking into consideration the DDCC non-idealities, the port relations in Eq. (1) can be expressed as:

\[ v_z = \beta_1 v_{y1} - \beta_2 v_{y2} + \beta_3 v_{y3} \] and \( i_z = \pm \alpha i_x \)  \hspace{1cm} \text{(9)}

where \( \beta_1 = 1 - \epsilon_v \), \( \beta_2 = 1 - \epsilon_{v2} \), \( \beta_3 = 1 - \epsilon_{v3} \) and \( \alpha = 1 - \epsilon_i \). Here \( \epsilon_{v1} (|\epsilon_{v1}| < 1) \) denotes the differential voltage tracking error of the DDCC from the \( y_1 \) terminal to the \( x \) terminal, \( \epsilon_{v2} (|\epsilon_{v2}| < 1) \) denotes the differential voltage tracking error of the DDCC from the \( y_2 \) terminal to the \( x \) terminal, \( \epsilon_{v3} (|\epsilon_{v3}| < 1) \) denotes the voltage tracking error of the DDCC from the \( y_3 \) terminal to the \( x \) terminal and \( \epsilon_i (|\epsilon_i| < 1) \) denotes the current tracking error from the \( x \) terminal to the \( z \) terminal of the DDCC. Reanalysis of the filter circuit in Fig. 1(a) yields

\[ A_{dm} = \frac{(\beta_1 + \beta_2)(-sCR_3 R_3 - R_2 + R_1 \alpha)}{2(sCR_3 + 1)(R_1 + R_2 - R_3 \beta_3)} \]  \hspace{1cm} \text{(10)}

![Fig. 1—The proposed DDCC based voltage-mode fully differential first-order allpass Filters](image-url)
\[ A_{cm} = \frac{(\beta_1 - \beta_2)(-sCR_2R_3 - R_2 + R_1\alpha)}{(sCR_1 + 1)(R_1 + R_2 - R_2\beta_1)} \quad \ldots (11) \]

The common-mode rejection ratio (CMRR) of this circuit can be found theoretically as:

\[ CMRR = 20\log_{10} \left| \frac{A_{dm}}{A_{cm}} \right| = 20\log_{10} \left| \frac{\beta_1 + \beta_2}{2(\beta_1 - \beta_2)} \right| \quad \ldots (12) \]

Then the designer must exercise special care for \( \beta_1 = \beta_2 \) to ensure the rejection of the common-mode voltage at the output.

The cutoff frequency is obtained by

\[ \omega_c = \frac{1}{CR_3} \quad \ldots (13) \]

The passive sensitivities are obtained as:

\[ S_{C}^{\alpha_1} = -1 ; \quad S_{R_1}^{\alpha_1} = -1 \]

Reanalysis of the filter circuit in Fig. 1(b) yields

\[ A_{dm} = \frac{(\beta_1 + \beta_2)(sCR_2R_3 + R_1\alpha - R_2)}{2(sCR_1R_2 + R_1 + R_2 - R_2\beta_1)} \quad \ldots (14) \]

\[ A_{cm} = \frac{(\beta_1 - \beta_2)(sCR_2R_3 + R_1\alpha - R_2)}{(sCR_1R_2 + R_1 + R_2 - R_2\beta_1)} \quad \ldots (15) \]

The CMRR of this circuit can be found theoretically as:

\[ CMRR = 20\log_{10} \left| \frac{A_{dm}}{A_{cm}} \right| = 20\log_{10} \left| \frac{\beta_1 + \beta_2}{2(\beta_1 - \beta_2)} \right| \quad \ldots (16) \]

Then the designer must exercise special care for \( \beta_1 = \beta_2 \) to ensure the rejection of the common-mode voltage at the output.

The cutoff frequency is obtained by

\[ \omega_c = \frac{R_1 + R_2 - R_2\beta_1}{CR_1R_2} \quad \ldots (17) \]

The active and passive sensitivities are obtained as:

\[ S_{C}^{\alpha_1} = -1 ; \quad S_{R_1}^{\alpha_1} = 0 ; \quad S_{R_2}^{\alpha_1} = -1 ; \quad S_{R_3}^{\alpha_1} = -\frac{R_3}{R_1} \]

**Simulation Results**

HSPICE simulations were carried out to demonstrate the feasibility of the proposed circuits using 0.18 µm, level 49 MOSFET from TSMC. The DDCC was realized by the CMOS implementation in Fig. 2 with the NMOS and PMOS transistor aspect ratios \( W/L=4.5\mu/0.9\mu \) and \( W/L=9\mu/0.9\mu \), respectively. The supply voltages are \( V_+ = +0.9 \text{ V} \), \( V_- = -0.9 \text{ V} \) and \( V_b = -0.38 \text{ V} \).

Figure 3 represents the simulated frequency responses for the fully differential first-order allpass filter of Fig. 1(a) designed with \( f_o = 318.3 \text{ kHz} \), \( C = 50 \text{ pF} \), \( R_1 = 5 \text{ k}\Omega \), \( R_2 = 5 \text{ k}\Omega \) and \( R_3 = 10 \text{ k}\Omega \). The maximum difference between the theoretical and the obtained pass-band gain is 0.349 dB. The obtained cutoff frequency is 324 kHz. The difference between the theoretical and the obtained cutoff frequency is 1.79%. Monte Carlo analyses with one hundred runs for 5% \( R_2 \) variations as the Gaussian distribution are given in Fig. 4. In Fig. 5, total harmonic distortion (THD) of the output signals are given at 318.3 kHz operation frequency. Figure 6 shows the square wave response.
Fig. 4—Monte Carlo analyses of Fig. 1(a) with one hundred runs for 5% $R_2$ variations as the Gaussian distribution (a) gain and (b) phase.

Fig. 5—THD analysis results of Fig. 1(a) with 150 mVp-p input at $V_{id}$ and $V_{od}$ output which confirms the stability of Fig. 1(a). Figure 7 represents the INOISE and ONOISE simulation results of Fig. 1(a) at $V_{od}$ output with $V_{i1} = 80$ mVp-p, $C = 50$ pF, $R_1 = 5$ kΩ, $R_2 = 5$ kΩ and $R_3 = 10$ kΩ.

Figure 8 represents the simulated frequency responses for the fully differential first-order allpass filter of Fig. 1(b) designed with $f_c = 318.3$ kHz, $C = 50$ pF, $R_1 = 5$ kΩ, $R_2 = 10$ kΩ and $R_3 = 5$ kΩ. The maximum difference between the theoretical and the obtained pass-band gain is 0.515 dB. The obtained cutoff frequency is 312 kHz. The difference between the theoretical and the obtained cutoff frequency is -1.98%. Monte Carlo analyses with one hundred runs for 5% $R_3$ variations as the Gaussian distribution are given in Fig. 9. In Fig. 10, total harmonic distortion (THD) of the output signals are given at 318.3 kHz operation frequency. Figure 11 shows the response of the filter of Fig. 1(a) with 150 mVp-p input at $V_{id}$ and $V_{od}$ output which confirms the stability of Fig 1(a). Figure 7 represents the INOISE and ONOISE simulation results of Fig. 1(a) at $V_{od}$ output with $V_{i1} = 80$ mVp-p, $C = 50$ pF, $R_1 = 5$ kΩ, $R_2 = 5$ kΩ and $R_3 = 10$ kΩ.

Fig. 6—Stability tests of the proposed filter in Fig. 1(a).

Fig. 7—INOISE and ONOISE simulation results of
Fig. 8—Simulated frequency responses of the proposed circuit in Fig. 1(b)

Fig. 9—Monte Carlo analyses of Fig. 1(b) with one hundred runs for 5% $R_f$ variations as the Gaussian distribution (a) gain and (b) phase

square wave response of the filter of Fig. 1(b) with 150 mV_{p-p} input at $V_{id}$ and $V_{od}$ output which confirms the stability of Fig. 1(b). Figure 12 represents the INOISE and ONOISE simulation results of Fig. 1(b)

Fig. 10—THD analysis results of Fig. 1(b)

Fig. 11—Stability tests of the proposed filter in Fig. 1(b)

Fig. 12—INOISE and ONOISE simulation results of Fig. 1(b)
at $V_{\text{od}}$ output with $V_{i1} = 80 \text{ mV}_{\text{pp}}$, $C = 50 \text{ pF}$, $R_1 = 5 \text{ k}\Omega$, $R_2 = 10 \text{ k}\Omega$ and $R_3 = 5 \text{ k}\Omega$.

Conclusions

Two voltage-mode fully differential first-order allpass filters each using one DDCC, one grounded capacitor and three resistors are presented. The proposed circuits have the advantage of high input impedance, using grounded capacitors and tunable of allpass gains. Tracking error analysis of the DDCC is included. The simulation results confirm the theoretical analysis.

Acknowledgements

The authors would like to thank the reviewers for their constructive suggestions to improve the manuscript. The first author would like to thank Dr Chun-Li Hou, who has always been a source of immense motivation and academic help. Dr Norbert Herencsar was supported by the projects CZ.1.07/2.3.00/30.0039 of Brno University of Technology and SIX CZ.1.05/2.1.00/03.0072 of the Operational Program Research and Development for Innovation.

References