Three-input-one-output current-mode universal biquadratic filter using one differential difference current conveyor

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A current-mode universal biquadratic filter is presented. The architecture has three input terminals, one output terminal using one differential difference current conveyor (DDCC), two grounded capacitors and two resistors. It can realize all standard second-order filter functions, which are, highpass, bandpass, lowpass, notch and allpass responses without changing the circuit topology. The proposed circuit employs only one DDCC that simplifies the circuit configuration.

\textbf{Keywords:} Current conveyor, Biquadratic filter, Active circuit, Current-mode

1 Introduction

There is a growing interest in designing current-mode current conveyor (CC) based active filters. This is attributed to their high signal bandwidths, greater linearity and larger dynamic range than OPAMP based ones\textsuperscript{1}. It is attractive for filters to employ grounded capacitors because of its easier monolithic IC implementation\textsuperscript{2,3}. Several current-mode universal biquadratic filters with multi-inputs have been presented\textsuperscript{4-11}. Chang and Chen\textsuperscript{4} proposed a current-mode universal biquadratic filter with three inputs and single output using five second-generation current conveyors (CCIIs), two grounded capacitors and six grounded resistors\textsuperscript{4}. Chang \textit{et al}\textsuperscript{5} proposed the second current-mode universal biquadratic filter with three inputs and single output using five second-generation current conveyors (CCIIs), two grounded capacitors and six grounded resistors\textsuperscript{5}. Chang\textsuperscript{6} proposed the third current-mode universal biquadratic filter with three inputs and single output using five plus-type CCIIs, two grounded capacitors and four grounded resistors\textsuperscript{6}. Chang and Tu\textsuperscript{7} proposed the fourth current-mode universal biquadratic filter with three inputs and single output using four multiple output CCIIs, two grounded capacitors and four grounded resistors\textsuperscript{7}. Gunes \textit{et al}\textsuperscript{8} proposed a current-mode universal biquadratic filter with four inputs and single output using three multiple output CCIIs, two grounded capacitors and two grounded resistors\textsuperscript{8}. Wang and Lee\textsuperscript{9} proposed a current-mode universal biquadratic filter with three inputs and three outputs using two multiple output CCIIs, one multiple output third-generation CC (CCIIII), two grounded capacitors and two grounded resistors\textsuperscript{9}. Horng\textsuperscript{10} proposed a current-mode universal biquadratic filter with five inputs and single output using three CCIIs, two grounded capacitors and three resistors. Horng \textit{et al}\textsuperscript{11} proposed a current-mode universal biquadratic filter with three inputs and single output using one CCI, one multiple output CCIII, two grounded capacitors and two grounded resistors.

Several current-mode universal biquadratic filters with five input terminals have been presented\textsuperscript{12-14}. However, the active or passive components used in the design of these multi-inputs current-mode universal filters\textsuperscript{4-14} were not minimum. Kacar \textit{et al}\textsuperscript{15} proposed a current-mode universal biquadratic filter with three inputs and single output using one fully differential current conveyor (FDCCI), two grounded capacitors and two grounded resistors\textsuperscript{15}. However, the FDCCI is a very complicated device. On each FDCCI, there are almost twice as many MOSs as one differential difference current conveyor (DDCC) needs. Moreover, the port relations of a FDCCI are equivalent to the port relations of two DDCCs arithmetically.

A new current-mode universal biquadratic filter with three inputs and single output using only one DDCC, two grounded capacitors and two resistors is
presented. The new current-mode circuit can realize all standard filter types. With respect to the multi-inputs current-mode biquads\(^4\)-\(^1\)\(^5\), the proposed circuit uses less active elements. With respect to the three inputs and single output current-mode biquad\(^1\)\(^5\), the proposed circuit uses simpler active device. A summary of these reported multi-inputs current-mode biquads\(^4\)-\(^1\)\(^5\) and the proposed filter are given in Table 1.

2 Circuit Description

Using standard notation, the port relations of a DDCC can be described by the following matrix equation\(^1\)\(^6\):

\[
\begin{bmatrix}
i_{y1} \\
i_{y2} \\
i_{y3} \\
v_x \\
i_{zk}
\end{bmatrix} = \begin{bmatrix}
0 & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & 0 \\
1 & -1 & 1 & 0 & 0 \\
0 & 0 & 0 & \pm 1 & 0
\end{bmatrix} \begin{bmatrix}
v_{y1} \\
v_{y2} \\
v_{y3} \\
v_x \\
v_{zk}
\end{bmatrix}
\]

where the plus and minus signs indicate whether the DDCC is configured as a non-inverting or inverting circuit, termed DDCC\(^+\) or DDCC\(^-\).

The proposed current-mode universal biquadratic filter is shown in Fig. 1. The circuit with three input terminals and one output terminal comprises one DDCC, two grounded capacitors and two resistors. The output current can be expressed as:

\[
I_{\text{out}} = \frac{s^2C_1C_2I_{\text{in}_3} - sC_2G_1I_{\text{in}_2}}{s^2C_1C_2 + s(C_2G_1 + C_1G_2 - C_1G_1) + G_1G_2}
\]

From Eq. (2), we can see that:

1. If \(I_{\text{in}_1} = I_{\text{in}_2} = 0\) (opened), then \(I_{\text{in}_3} = \) input current signal, a highpass filter can be obtained with \(I_{\text{out}}/I_{\text{in}_3}\).
2. If \(I_{\text{in}_1} = I_{\text{in}_3} = 0\) (opened), then \(I_{\text{in}_2} = \) input current signal, a bandpass filter can be obtained with \(I_{\text{out}}/I_{\text{in}_2}\).

<table>
<thead>
<tr>
<th>Ref.</th>
<th>No. of active devices</th>
<th>No. of passive elements</th>
<th>Matching constraints</th>
<th>Low input impedance</th>
<th>High output impedance</th>
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<tr>
<td>[4]</td>
<td>5 CCIIs</td>
<td>6R/2C</td>
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<td>no</td>
<td>yes</td>
</tr>
<tr>
<td>[5]</td>
<td>4 CCs</td>
<td>2R/2C</td>
<td>no</td>
<td>no</td>
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</tr>
<tr>
<td>[6]</td>
<td>5 CCH+s</td>
<td>4R/2C</td>
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<td>no</td>
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</tr>
<tr>
<td>[7]</td>
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<td>4R/2C</td>
<td>yes</td>
<td>no</td>
<td>yes</td>
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<tr>
<td>[8]</td>
<td>3 CCIIs</td>
<td>2R/2C</td>
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<td>no</td>
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</tr>
<tr>
<td>[9]</td>
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<td>no</td>
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</tr>
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<td>[10]</td>
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<td>3R/2C</td>
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<tr>
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<tr>
<td>[12]</td>
<td>2 CCIIs</td>
<td>3R/2C</td>
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<td>no</td>
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<td>[13]</td>
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<td>2R/2C</td>
<td>no</td>
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<td>3R/2C</td>
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<td>2R/2C</td>
<td>yes</td>
<td>no</td>
<td>no</td>
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</table>

Fig. 1 — Proposed universal filter
3 Analysis of Sensitivities

Taking the non-idealities of the DDCC into account, the relationship of the terminal voltages and currents of DDCC can be rewritten as:

\[
\begin{bmatrix}
i_1 \\
i_2 \\
i_3 \\
i_{Gk}
\end{bmatrix} = \begin{bmatrix}
0 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 \\
0 & 0 & 0 & \pm \beta_k(s)
\end{bmatrix} \begin{bmatrix}
v_1 \\
v_2 \\
v_3 \\
v_{Gk}
\end{bmatrix}
\]

where \( \alpha_k(s) \) represents the frequency transfer function of the internal voltage follower and \( \beta_k(s) \) represents the frequency transfer function of the internal current follower of the DDCC. They can be approximated by first order lowpass functions, which can be considered to have a unity value for frequencies much lower than their corner frequencies. If the circuit is working at frequencies much lower than the corner frequencies, then \( \alpha_k(s) = \alpha_k = 1 - \varepsilon_{ik} \) and \( \beta_k(s) = \beta_k = 1 - \varepsilon_{ki} \). The voltage tracking error from \( y_k \) terminal to \( x \) terminal of the DDCC and \( \varepsilon_k = \varepsilon_{kk} \), \( \varepsilon_{ik} \) and \( \varepsilon_{ki} \) denotes the current tracking error from the \( x \) terminal to \( z_k \) terminal of the DDCC. The denominator of the non-ideal output current function for Fig. 1 becomes:

\[
D(s) = s^2 C_1 C_2 + s(C_2 G_1 \alpha_3 \beta_2 + C_1 G_2 - C_1 G_1 \alpha_1 \beta_1) + G_1 G_2 \alpha_3 \beta_3
\]

The resonance angular frequency \( \omega_o \) and quality factor \( Q \) become:

\[
\omega_o = \frac{G_1 G_2 \alpha_3 \beta_3}{C_1 C_2}
\]

\[
Q = \frac{\sqrt{C_1 C_2 G_1 G_2 \alpha_3 \beta_3}}{C_1 G_1 \alpha_1 \beta_1}
\]

The active and passive sensitivities of \( \omega_o \) and \( Q \) are shown as:

\[
S_{\omega_o} = -S_{Q} = \frac{1}{2}
\]
\[ S_{G_1}^Q \equiv \frac{C_1 G_1 + C_2 G_2 - C_1 G_1}{2(C_2 G_1 + C_1 G_2 - C_1 G_1)} \]
\[ S_{G_2}^Q \equiv \frac{C_1 G_1 + C_2 G_2 - C_2 G_1}{2(C_2 G_1 + C_1 G_2 - C_1 G_1)} \]
\[ S_{G_2}^Q \equiv \frac{C_2 G_1 + C_1 G_2 - C_1 G_1}{2(C_2 G_1 + C_1 G_2 - C_1 G_1)} \]
\[ S_{\alpha_{\beta}}^Q \equiv \frac{C_1 G_1}{C_2 G_1 + C_1 G_2 - C_1 G_1} \]
\[ S_{\alpha_{\beta}}^Q \equiv \frac{C_1 G_1 - C_1 G_1 - C_2 G_1}{2(C_2 G_1 + C_1 G_2 - C_1 G_1)} \]

**4 Effect of Parasitic Elements**

A non-ideal non-inverting type DDCC model\(^{18}\) is shown in Fig. 2. It is shown that the real DDCC has parasitic resistors and capacitors from the \(y_1, y_2, y_3\) and \(z_2\) terminals to the ground, and also, a series resistor at the input terminal \(x\). Taking into account the non-ideal DDCC and assuming the circuit is working at frequencies much lower than the corner frequencies of practical DDCC, the external resistors can be chosen to be much greater than the parasitic resistors at the \(y\) and \(z\) terminals of DDCC and much greater than the parasitic resistor at the \(x\) terminal of DDCC, i.e. \(R_x, R_z\)

\[ \omega >> R_x >> R_z. \]

The external capacitances \(C_1\) and \(C_2\) can be chosen to be much greater than the parasitic capacitors at the \(y\) and \(z\) terminals of DDCC, i.e. \(C_y, C_z << C_1, C_2\). Under these conditions, the output current of Fig. 1 becomes:

\[ [s^2 C_1^2 + s(C_2 G_a + C_1^2 G_2 - C_1 G_2)] \]
\[ + G_2 G_2 - G_2 G_a]\]
\[ - (sC_2 G_1 + G_1 G_2 - G_1 G_2) I_{in2} \]
\[ I_{out} = \frac{s^2 C_1^2 C_2^2 + s(C_2 G_a + C_1^2 G_2 - C_1 G_2)}{s^2 C_1^2 + s(C_2 G_a + C_1^2 G_2 - C_1 G_2)} \]
\[ + G_2 G_2^2 \]

where \(C_1 = C_1 + C_y, C_2 = C_2 + C_y, G_2 = G_2 + G_y + G_z, G_1 = G_1 + G_z\).

In Eq. (12), undesirable factors are yielded by the non-idealities of the DDCC. The conductances \(G_a, G_1\) and \(G_a\) become non-negligible at very low frequencies. To minimize the effects of the DDCC’s non-idealities, the operation angular frequency should be restricted to the following conditions:

\[ \omega >> \max \left\{ \frac{C_2 G_a + C_1^2 G_2 - C_1 G_2}{C_1^2 C_2}, \frac{C_1 G_2 - G_2 G_a}{C_1^2 C_2}, \frac{G_1 G_2 - G_1 G_2}{C_1^2 C_2}, \frac{G_1 G_2}{C_1^2 C_2} \right\} \]
\[ \omega >> \frac{G_2 G_2}{C_1^2 (G_2 - G_1)} \]

**5 Simulation Results**

HSPICE simulations were carried out to demonstrate the feasibility of the proposed circuit in Fig. 1 using 0.18 \(\mu\)m, level 49 MOSFET from TSMC. The DDCC was realized by the CMOS implementation\(^{17}\) in Fig. 3. The dimensions of the NMOS transistors in the DDCC are set to be \(W = 4.5 \mu\)m and \(L = 0.9 \mu\)m. The dimensions of the PMOS transistors in the DDCC are set to be \(W = 9 \mu\)m and \(L = 0.9 \mu\)m. The supply voltages are \(V_+ = +0.9\) V, \(V_+ = -0.9\) V, \(V_{b1} = -0.38\) V and \(V_{b2} = 0.28\) V. Figure 4 shows the simulated frequency responses for the highpass filter of Fig. 1 designed with \(I_{a3} = I_{a4}, I_{a3} = I_{a4} = 0\), \(C_1 = C_2 = 10\) pF, \(R_1 = 10\) k\(\Omega\) and \(R_2 = 10\) k\(\Omega\). Figure 5 shows the simulated frequency responses for the bandpass filter of Fig. 1 designed with \(I_{a2} = I_{a3}, I_{a2} = I_{a3} = 0\), \(C_1 = C_2 = 10\) pF, \(R_1 = 10\) k\(\Omega\) and \(R_2 = 10\) k\(\Omega\).
Comparisons between the theoretical and simulated results for the highpass filter in Fig. 1

Comparisons between the theoretical and simulated results for the bandpass filter in Fig. 1

Comparisons between the theoretical and simulated results for the lowpass filter in Fig. 1

Figure 6 shows the simulated frequency responses for the lowpass filter of Fig. 1 designed with $I_{in1} = I_{in1}$, $I_{in2} = I_{in2} = 0$, $C_1 = C_2 = 10 \text{ pF}$, $R_1 = 10 \text{ k}\Omega$ and $R_2 = 10 \text{ k}\Omega$. Figure 7 shows the simulated frequency responses for the notch filter of Fig. 1 designed with $I_{in1} = I_{in3} = I_{in}$, $I_{in2} = 0$, $C_1 = C_2 = 10 \text{ pF}$, $R_1 = 10 \text{ k}\Omega$ and $R_2 = 10 \text{ k}\Omega$. Figure 8 shows the simulated frequency responses for the allpass filter of Fig. 1 designed with $I_{in1} = I_{in2} = I_{in3} = I_{in}$, $C_1 = C_2 = 10 \text{ pF}$, $R_1 = 10 \text{ k}\Omega$ and $R_2 = 10 \text{ k}\Omega$. If all input currents are opened, the power dissipation is 159.887 $\mu$W. The lowpass filter requires resistances matching conditions. When the parasitic elements of the DDCC are taking into account, it may introduce zeros at high frequency from Eq. (12). This can explain why Fig. 6
Fig. 7 — Comparisons between the theoretical and simulated results for the notch filter in Fig. 1

Fig. 8 — Comparisons between the theoretical and simulated results for the allpass filter in Fig. 1

Fig. 10 — THD analysis results of the proposed bandpass filter

has non-ideal responses at high frequencies. To reduce the effect of this zero, more accurate DDCC CMOS circuits maybe required for this circuit in lowpass filter applications.

Figure 9 shows the input and output signals of bandpass response designed with $I_{in2} =$ input current signal, $I_{in1} = I_{in3} =$ 0 (opened) and $Q = 1: C_1 = C_2 = 10 \text{ pF, } R_1 = 10 \text{ k}\Omega$ and $R_2 = 10 \text{ k}\Omega$. It is observed that 1.6423 MHz with 17 $\mu$Ap-p input current signal levels are possible without significant distortion. In Fig. 10, total harmonic distortion (THD) of the bandpass signals are given at 1.6423 MHz operation frequency.

6 Conclusions
Several current-mode multi-inputs universal biquadratic filters were proposed in the literature. However, the active components constructed in these biquads were not minimum. A current-mode three inputs biquad was proposed. However, it employs a very complicated device (FDCCII).

In this paper, a new universal biquadratic current filter with three inputs and single output using only one DDCC, two grounded capacitors and two resistors is presented. The proposed circuit can synthesize any type of filter transfer functions. The proposed circuit employs less active elements with respect to the previous filters. The proposed circuit employs simpler active device (DDCC) with respect to the previous biquad.

References