Minimizing switching activities through reordering algorithm for efficient power management

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One of the emerging challenges in the current scenario of modern-day technologies is the power dissipation occurring in high end VLSI circuits that are predominantly caused due to the switching activities of the circuit under test procedures. We have presented a well-organized test pattern generator that is more appropriate for built in self-test (BIST) structures used in the testing of VLSI circuits. The BIST sufficiently keeps the power dissipation in check without altering the fault coverage. Our version of the test pattern generator aims at bringing down the switching activity to the least minimum amount possible. In addition to this, a modified version of Floyd algorithm is used which re-orders the vectors in the test sequence and this further reduces the switching activities that occurs while testing of combinational circuits. This technique brings down the hamming distance between test vectors which leads to reduction in dynamic power dissipations to a great extent. Moreover, in order to reduce execution time and power, genetic algorithm is incorporated with Floyd algorithm. We have used the ISCAS’85 benchmark circuit for our experiments.

Keywords: Hamming distance, power dissipation, switching activity, re-ordering, Floyd algorithm.

Introduction

More and more portable computing devices are coming up every year and manufacturers crave for more battery up-time and this is what we have tried to satisfy with our methods presented in this paper. The major factors that affect battery up-time and its life are excessive power dissipation in the form of heat under heavy workloads. Hence a reduction in this power dissipation and maintaining a moderate temperature within the circuits help prolong battery runtime and its life and also minimizing the package size of the batteries become feasible1. In general, the power dissipation of a system in test mode is more than in normal mode2. Surges in power consumption occur mainly due to high switching activities from minimally correlated test vectors3.

The average and peak power consumption create problems like instantaneous power surge which results in circuit damage and sometimes results in the formation of hot spots, complexities in performance verification, reduction of the product field and life time4. Therefore, we had to make sure that the power ratings specified in the circuits are not exceeded during test applications. When the circuit was tested with pseudo random patterns, we found that consecutive input test vectors are statically independent that resulted in increased switching activity. Since in CMOS circuits, energy is majorly consumed by signal transition, the average power consumption during testing is comparatively higher than normal mode of operation5. The relationship between hamming distance6 and the average power of the circuit plays a vital role in reducing the test power. More methods have developed over time to reduce this type of power consumption.

LT-TPG claims to reduce the average and peak power of a circuit under test7. A better low power can be attained by using a single input change pattern generator. It was proposed that the combination of LFSR and scan shift register can be used to generate random single input charge sequences8. In9 we stated that \((2^m-1)\) single input changing data is inserted between two neighboring seeds. The average and peak power are optimized by using the before mentioned techniques. The average and peak power are optimized by using the before mentioned techniques. Still, the switching activities will be significantly high when clock frequency is high.

Also, various techniques are available to reduce the switching activities of test pattern, which decrease

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power consumption in test mode. Authors proposed new ATPG (Automatic Test Pattern Generation) techniques\textsuperscript{10} which reduce the power dissipated during test application in addition to the normal ATPG objectives. Santanu chattopadhyay proposed a technique based on Genetic algorithm\textsuperscript{11} to reduce the testing power. The author\textsuperscript{12} evolved the methods for re-ordering the test vectors to minimize dynamic power dissipation of the circuits under test. In paper\textsuperscript{13}, authors mentioned about the reordering sequences of completely specified test patterns. Linear feedback shift registers [LFSR] are used a lot for the test pattern generations as it is a very simple circuit and also as it occupies less area. The method of reordering of test patterns is achieved through graph theory concept\textsuperscript{8, 14}. In this paper, in contrast to that, we have proposed a technique based on hamming distance between the successive test patterns. A modified Floyd algorithm is utilized to find the best solution for reordering the test sequences. The rest of the paper explains an overview of power analysis for testing, the proposed techniques and experimental results.

**Analysis of Power for Testing**

In CMOS technology, the power dissipation can occur in two manners, which can be either static or dynamic. Static power dissipation happens due to unintentional leakage of current. Dynamic power dissipation is caused by switching transient current and charging and discharging of load capacitances. Some important parameters for evaluating the power consumption of CMOS circuits are discussed below.

\[
e_i = \frac{1}{2} V_{dd}^2 C_0 F_i S_i \quad \ldots (1)
\]

Where, \( C_0 \) is the load capacitance, \( V_{dd} \) is the supply voltage. The product of \( F_i \) and \( S_i \) gives the weighted switching activity of internal circuit node \( i \). The overall power consumption by an internal circuit node \( I \) can be represented by,

\[
P_i = \frac{1}{2} V_{dd}^2 C_0 F_i S_i f \quad \ldots (2)
\]

Where, \( f \) is the clock frequency. The summary of \( P_i \) of all the nodes is named as average power consumption. It can be observed from (1) and (2) that the energy and power consumption are mainly due to the switching activities, clock frequency and supply voltage. We aim at reducing the switching activity at the inputs of the circuit under test (CUT) to a level as low as possible.

**Proposed Methodology**

Generally test patterns produced from pseudo random pattern generator are random in nature and so the switching activity is larger when those patterns are applied as input to the circuit. During testing, the power dissipation is more and that can be reduced by minimizing the number of transitions in the circuit under test.

The low power test pattern generator consists of modified LFSR, m-bit counter, gray counter, NOR-gate structure and XOR-array. The m-bit counter is initialized with zeros and which generates \( 2^m \) test patterns in sequence. The output of m-bit counter is taken as input to gray code generator and NOR-gate structure. The NOR-gate output is one when all the bits of counter output are zero. Only when the NOR-gate output is one, the modified clock signal is applied to modified LFSR which generates the next seed. The seed generated from the modified LFSR is XOR-ed with the data generated from gray code generator. The output patterns are taken from the exclusive–or array.

The modified LFSR consists of D-flipflops and multiplexers. Multiplexers are used to exchange the output of adjacent flip flops. The output of last flip flop is considered as a select line. If the output of the last flip flop (select line) is one, the swapping operation will be carried out between the selected adjacent flip flop outputs. If the output of the last flip flop (select line) is zero, no swapping will be carried out. The output from other flip flops will be taken as such. In this way, the low power test pattern generator generates the test patterns with low power; in addition to that, the number of transitions can be reduced by decreasing the hamming distance between the consecutive test vectors. The hamming distance can be reduced to a large extent during testing. The problem of reducing the power dissipation due to switching activity can be solved by Graph theory using Hamiltonian path technique, in which test vectors are considered as node and hamming distance between them are considered as edge cost. Reordering algorithm is applied to determine the Hamiltonian path, which provides the resultant reordered test vector whose hamming distance is very less.
Another solution to reduce the hamming distance is based on Floyd’s algorithm\cite{15-17}, which is mainly used to find the least expensive paths between all the vertices in a graph. It is carried out by operating on a matrix which represents the cost of edges between vertices. A matrix in a two-dimensional array should be developed to invoke Floyd’s algorithm. Each row in the matrix represents a starting vertex in the graph while each column represents an ending point in the graph. Here, each vertex is considered as test vector. Once the matrix is constructed, the Floyd’s algorithm is used to compute the less switching activity between all the points in the graph. When the Floyd’s algorithm is executed, the entries in all the positions of matrix will be updated which represent the lowest hamming distance between the row test vector and column test vector. This reordered test vector sequence offers less number of transitions at the input which in turn results in minimum power dissipation in the circuit during testing.

The following are the steps involved in the developed algorithm to minimize the hamming distance.

- Our modification of Floyd Algorithm involves recursive function of all possible states of hamming distance, whether it is 4-bit or 8-bit series. For the given 16 numbers (4-bit or 8-bit), we permute all the possible order of arranging those 16 numbers.
- For the very first permuted order, we determine the hamming distance and then both the order of numbers and the hamming distance are stored in the memory.
- Then we take in the second order and while it’s hamming distance is being calculated, is compared with the previously stored hamming distance value.
- During the process if in case the second order hamming distance equals the stored hamming distance, then its evaluation is terminated and moved to the next order.
- If the evaluated hamming distance is smaller than the stored value, then the present order and hamming distance is replaced with the stored value.
- Then it is compared with the third sequence and the process goes on.
- At the end it results in the order with least hamming distance.

The results from this method can be proven to be the best one, since it takes into consideration all the possible combinations. In addition to that, the genetic algorithm is also incorporated with Floyd algorithm for further improvement as explained below. Test pattern sequences are given as input parameters to the Floyd algorithm and the process will be carried out. While doing the process, if it encounters any ambiguity problem, two or more iterations passed to the genetic algorithm. After processing those data, genetic procedure will return a single iteration that is selected and given as input to Floyd algorithm procedure and these processes iteratively performed until complete data is arranged in the manner to reduce switching transitions.

Procedure-Genetic:
1. Input: Receive two or more suitable Iterations and secondary iteration layer.
2. Apply crossover for input iterations.
3. Verify data convergence based on fitness function.
   Fitness function: $\exists dx, dx+1 | [dx, dy] = 0$
   Checking convergence path is verified and decision is made in the following step.
4. Check node count=2048 (2K)
   If node count=2048, verify convergence path is in optimal direction.
   If YES: Proceed crossover to the current stream and reset node count to 0.
   If NO: Apply one mutation.
5. Repeat the procedure to get the optimum result of fitness function.

Results and discussions
To exhibit the efficiency of the proposed approach, we have performed experiments on 4-bit, 6-bit, 7-bit, 8-bit linear feedback shift registers, and low power test pattern generator with normal linear feedback shift register and low power test pattern generator with modified linear feedback shift register. Also to verify the methodology, 4-bit and 8-bit multipliers are taken as circuit under test and the test patterns generated from 4-bit and 8-bit LFSR are given as input to the multipliers, and later the generated test patterns are reordered and once again given as inputs to the multipliers. The Floyd with genetic algorithm has been implemented in visual C++ with Xilinx ISE 9.1i as supporting software. We used the ISCAS’85 benchmark circuits for our experiment.
The test patterns generated from the aforementioned architectures are applied to the Floyd algorithm to obtain the optimal reordered test patterns with less number of switching transitions. The Floyd algorithm is developed using visual C++. Table 1 shows the total hamming distance reduction (THD) when the test patterns are reordered using Floyd algorithm. To authenticate the efficacy of the proposed method, the generated reordered test patterns are applied to test the synchronous pipelined 4×4 and 8×8 Braun array multipliers. Table 3 denotes the power analysis of circuit under test. Fig. 1 shows the analysis of switching transitions. Fig. 2 shows the analysis of dynamic power dissipation. Simulation and analysis were carried out with QUARTUS-II 9.1 version. Power play power analyzer tool was used for the Power analysis. Table 2 illustrates the analysis of switching transitions between reordered and unordered test patterns. Table 4 shows the switching transitions, power and time of modified Floyd and Floyd integrated with genetic algorithms.

**Conclusion**

In VLSI design, power dissipation has been a major issue during testing. The low power design in VLSI circuits demands various approaches for the test power optimization. Various techniques have been discussed so far to reduce the switching activities upon the test patterns generated from the patterns generator. An algorithm for the test power optimization has been proposed in this paper. Since the 80% of the total power dissipation in CMOS circuits is due to the switching activity, the proposed algorithm reduces the switching activity by reordering the sequence of test vectors of the CUT. A low power test pattern generator has been proposed with a modified LFSR along with reordering algorithm to

![Fig. 1 – Analysis of switching transitions](image1.png)

![Fig. 2 – Analysis of dynamic power dissipation](image2.png)

<table>
<thead>
<tr>
<th>Table 1—Total Hamming Distance (THD) Reduction</th>
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<tr>
<td>Size of LFSR</td>
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<tr>
<td>THD without ordering</td>
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<td>THD with ordering</td>
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<th>Table 2—Analysis of Switching Activity</th>
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<td>Design of LFSR</td>
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<tr>
<td>4 bit LFSR</td>
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<td>Low power test pattern generator with modified LFSR</td>
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<td>8 bit LFSR</td>
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The seed generated from LFSR is XOR-ed with the single input changing sequences generated from gray code generator, which efficiently reduces the switching activities among the test patterns. A modified Floyd algorithm has been proposed which appreciably reduces dynamic power dissipation during testing. Also the genetic algorithm integrated with Floyd increases the speed of the system and reduces the power to a significant level.

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**References**


