Empirical model for temperature dependent threshold voltage and drain current-voltage characteristics of thin film short-channel SOI MOSFETs

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The temperature dependence of threshold voltage and drain-source current of thin film SOI MOSFET's has been investigated and modeled for a non-uniform distribution in the silicon film, taking into account the field dependent mobility, and fringing field effects near the drain and source ends. A decrease in threshold voltage and drain current with increase in temperature is established. The predictions of the model are in good agreement with the experimental data. The model is valid for both short-channel and long-channel devices.

1 Introduction

Evaluation of temperature dependence of the device characteristics is important for designing scaled down MOS integrated circuits that generally operate over a wide range of temperatures. The use of bulk MOSFET's in the high temperature range is limited by the latch-up due to the increased leakage current through the well junction. SOI MOSFET circuits do not contain n or p wells, which are the primary causes of leakage in bulk circuits operating at elevated temperatures. This leads to a practical need for a temperature dependent SOI MOSFET model for circuits and device simulation even if it contains few empirical parameters. The temperature dependence of threshold voltage on thick film has been studied by several workers and significant effect is observed. Recently it was observed in thin film long channel devices that the threshold voltage depends on the depletion level, which in turn is temperature dependent.

Assuming a gaussian doping profile, we present an accurate temperature dependent model for threshold voltage and drain current-voltage characteristics of short-channel SOI MOSFETs. The model is an extension of the short-channel threshold voltage model. The silicon bandgap, built-in-potential, Fermi potential, flat band voltage, intrinsic carrier concentration and field dependent mobility are the key temperature dependent parameters. The model includes technology dependent empirical constants whose values are determined by curve fitting the experimental data. The model is valid in the enhanced range (25°C ≤ T ≤ 200°C) of temperature. The obtained results are in good agreement with experimental data which confirm the validity of the model.

2 Model

Cross-sectional view of an n-channel enhancement mode fully depleted SOI MOSFET is shown in Fig. 1, where Vgs is the gate source voltage and Vds is the drain source voltage.

2.1 Temperature dependence of Band gap, intrinsic carrier concentration

The temperature dependence of bandgap, \( E_g \) and intrinsic carrier concentration, \( n_i \), is given by

\[
E_g = 1.206 - 2.73 \times 10^{-3} T \quad (1)
\]

and

\[
n_i = 3.74 \times 10^{25} T^{1.5} \exp \left( \frac{-1.206}{2kT} \right) \quad ; \quad T \geq 250K \quad (2)
\]
respectively.

Fig. 1 – Cross-sectional view of an n-channel enhancement mode fully depleted SOI MOSFET. The shaded area shows the depletion region.

The expressions for built-in-potential, φ_b and Fermi potential, φ_f are

\[ \phi_b = \frac{E_x}{2} + \frac{kT}{q} \ln \left( \frac{N_A(x)}{n_i} \right) \] (3)

and

\[ \phi_f = \frac{kT}{q} \ln \left( \frac{N_A(x)}{n_f} \right) \] (4)

respectively.

Due to thermal oxidation, the impurity redistribution in thin silicon film results in a non-uniform distribution resembling a Gaussian distribution of the form given by

\[ N_A(x) = \frac{Q}{\sigma \sqrt{2\pi}} \exp \left[ -\frac{(x-R_p)^2}{2\sigma^2} \right] \] (5)

where Q, R_p, \sigma are the channel implant dose, projected range, and standard deviation respectively. Their values are listed in Table 1.

2.2 Temperature dependence of threshold voltage

Threshold voltage of short-channel SOI MOSFETs is given by (See Appendix)
\[
A = \left( \frac{\left( \phi_n + \sigma_1 \right) - \left( \phi_n + \sigma_1 + V_{\text{so}} \right) \exp \left( -\Gamma_{\text{ef}} \right)}{1 - \exp \left( -2\Gamma_{\text{ef}} \right)} \right) \]
\[
b = \left( \frac{\left( \phi_n + \sigma_1 + V_{\text{so}} \right) - \left( \phi_n + \sigma_1 \right) \exp \left( -\Gamma_{\text{ef}} \right)}{1 - \exp \left( -2\Gamma_{\text{ef}} \right)} \right) \exp \left( -\Gamma_{\text{ef}} \right) \]
\[
\Gamma_{\text{ef}} = L_{\text{ef}} \sqrt{\frac{\alpha}{\epsilon}} \]
\[
\alpha_j = \frac{\beta_j}{\alpha_0}, \quad \alpha_j = 2 \left( \frac{1 + \alpha_j}{f} \right) \]
\[
a = \frac{C_h}{C_s} + \frac{C_i}{C_s} : \quad f = \left( t_{\text{g}} \right)^2 \left[ 1 + 2 \frac{C_h}{C_s} \right] \]
\[
\beta_j = \frac{qN_{\text{A}}(0)}{\epsilon_{\text{ox}}} - \beta \]
\[
\beta = \frac{2}{f} \left( \alpha V'_{\text{so}} + V'_{\text{so}} \right) \]

Here, \( t_s \) is the silicon film thickness, \( t_i \) is the oxide thickness, \( t_o \) is the buried oxide thickness, \( \epsilon_s \) is dielectric permittivity for silicon and \( \epsilon_{so} \) is dielectric permittivity for oxide. \( V_{\text{so}} \) is the drain-source voltage, \( V_{\text{so}} \) is the gate-source voltage and \( V_{\text{so}} \) is the substrate voltage. \( V_{\text{so}} \) is front gate flatband voltage and \( V_{\text{so}} \) is the backgate voltage. \( L_{\text{ef}} \) is the effective channel length of the device.

A new temperature dependent empirical parameter \( t_d \) is introduced in the model. The empirical constants \( a, b \) and \( c \) are technology dependent whose values are determined by curve fitting the experimental data. Their values are listed in Table 2. The backgate oxide capacitance, \( C_h \), in the present model, is not neglected in comparison to \( C_s \) and \( C_h \), leading to modified definitions of \( \sigma_1, \alpha_0 \) and \( \beta_j \) given by Eqs (15), (16) and (18) respectively.

We express short-channel threshold voltage as an explicit function of temperature in Eq. (6b). It is evident from Eq. (6b) that \( \partial V_{\text{th}} / \partial T \) is not simply \( \partial \varphi_{\text{so}} / \partial T \) but higher and involves quite a complex dependence on temperature. The value of \( \partial V_{\text{th}} / \partial T \) for the present model is found to be \(-0.83 \, \text{V} \) for \( t_t = 19 \, \text{nm} \) and \( N_d(0) = 1.6 \times 10^{19} \, \text{m}^{-3} \) at \( T = 20 \, \text{C} \) which matches with the one extracted from the experimental data shown in the threshold voltage-temperature graph for thin film device. The variation of threshold voltage with temperature is shown in Fig. 2. Both Fermi potential and flat band voltage reduce with rise in temperature irrespective of \( n \) or \( p \) channel devices. This results in threshold voltage reduction at higher temperatures. At \( V_{\varphi} = 0 \), some field lines, originating from the source and drain, terminate at the bulk charges in the channel region. This effect reduces the effective depletion charge controlled by the gate leading to a prominent threshold voltage reduction for short-channel devices. This effect is being taken care of in the present model. For \( V_{\varphi} > 0 \), the depletion region near the drain expands further and results in greater reduction of the effective charge with different temperatures. The model is compared with the experimental data available in the literature and is found to be in perfect harmony. This validates the present model in temperature scenario.

### Table 1 - Technological parameters used in the model

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Values</th>
</tr>
</thead>
<tbody>
<tr>
<td>( T_{\text{d}} )</td>
<td>300 K</td>
</tr>
<tr>
<td>( E_{\text{d}} )</td>
<td>( 8.25 \times 10^{-12} , \text{V} )</td>
</tr>
<tr>
<td>( \sigma_{\text{d}} )</td>
<td>( 3.4 \times 10^{-2} , \mu \text{m} )</td>
</tr>
<tr>
<td>( \sigma )</td>
<td>( 2.86 \times 10^{-2} , \mu \text{m} )</td>
</tr>
<tr>
<td>( \epsilon_{\text{so}} )</td>
<td>( 3.4 \times 10^{-9} , \mu \text{m} )</td>
</tr>
<tr>
<td>( \epsilon_{\text{so}} )</td>
<td>( 3.4 \times 10^{-9} , \mu \text{m} )</td>
</tr>
<tr>
<td>( V_{\text{so}} )</td>
<td>( 1.04 \times 10^{-6} , \text{V} )</td>
</tr>
<tr>
<td>( V_{\text{so}} )</td>
<td>( 1.04 \times 10^{-6} , \text{V} )</td>
</tr>
</tbody>
</table>

2.3 Temperature dependence of drain current

The drain current in the conducting channel is computed by including the temperature dependence of built-in-potential, intrinsic carrier concentration, effective electron mobility, \( \mu_{\text{so}} \), critical electric field, \( E_c \) and inversion layer charge, \( Q_{\text{in}}(y) \) in the model. The drain current for strongly inverted \( n \)-channel enhancement mode SOI device is given by

\[
I_{d} = W \mu_{\text{eff}}(y) Q_{\text{s}}(y) \left( \frac{d\Phi_f(y)}{dy} \right) \]

\[\text{... (20)}\]
temp: \[ C \] 
width: \[ W \]

\[ \mu_{\text{eff}}(y) = \frac{\mu_{\text{sat}} \left( \frac{T}{T_0} \right)^{1/6}}{1 + \left( \frac{E_r(y)}{E_c} \right)} \]  \hspace{1cm} \text{(21)}

where \( E_r(y) \) is the normal electric field at the front surface, \( \mu_{\text{sat}} \) is the electron mobility at zero electric field and \( E_c \) is the critical electrical field whose value is given in Table 1.

The inversion layer charge density is calculated as
\[ Q_i(y) = Q_s(y) - Q_b \]  \hspace{1cm} \text{(22)}

where \( Q_s(y) \), the surface charge density is
\[ Q_s(y) = -C_f(\Phi_i(y) - V_{th}) \]  \hspace{1cm} \text{(23)}

The threshold voltage can also be expressed as
\[ V_{th} = V_{th0} + \Phi_i \frac{Q_p}{C_f} \]  \hspace{1cm} \text{(24)}

Comparison of Eq. 6(a) and Eq. 24 yields an expression for depletion layer charge density, \( Q_p \)

\[ Q_p = -qN_{\lambda}(0)t_{ox} + (V_{th0} - V_{ps})C_h + \]
\[ \frac{C + d - \Phi_i}{1 - E} + C_f \Phi_i \]  \hspace{1cm} \text{(25)}

Substituting Eq. (21), (23) and (25) in Eq. (20) and integrating from source to drain, an explicit expression for drain current is obtained
\[ I_{dh} = MF_c \left[ F_1 \left( \ln \left( \frac{1 + \lambda - \ln(1 + \lambda)}{E_r + V_{th0}} \right) \right) \right] \]  \hspace{1cm} \text{(26)}

where
\[ \lambda = \frac{M}{C_f \left( \Phi_i(y) - V_{th} \right)} \]  \hspace{1cm} \text{(27)}

\[ F_2 = 1 - V_{th} \frac{d^*}{d'} ; \quad F_1 = e^{\frac{X}{T_0}} \]  \hspace{1cm} \text{(28)}

\[ F_c \] is an additional temperature dependent empirical parameter. The values of technology dependent empirical constants \( a', b', c', \) and \( d' \) are extracted from (Fig. 3) the experimental data and are listed in Table 2.

<table>
<thead>
<tr>
<th>Empirical constants</th>
<th>Values</th>
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<tr>
<td>( a' )</td>
<td>0.57</td>
</tr>
<tr>
<td>( b' )</td>
<td>0.40</td>
</tr>
<tr>
<td>( c' )</td>
<td>3.00</td>
</tr>
<tr>
<td>( d' )</td>
<td>0.38</td>
</tr>
<tr>
<td>( e' )</td>
<td>0.65</td>
</tr>
<tr>
<td>( f' )</td>
<td>1.45</td>
</tr>
<tr>
<td>( g' )</td>
<td>1.55</td>
</tr>
</tbody>
</table>
Fig. 3—Drain current-voltage characteristics for SOI MOSFET with $t_{si}=50$ nm.

$L_{sd}=0.5 \mu m$, $N_{A}(x)=6 \times 10^{15} m^{-2}$, $Q=9 \times 10^{15} m^{-4}$ and $V'_{sc}=2V$.

(-----) Calculated; (● ● ●) experimental

Fig. 4 shows the drain current-voltage characteristics for three different temperatures. It is seen that drain current reduces at higher temperatures. The reason is that the channel mobility degrades due to the increased phonon scattering at higher temperature. Surface scattering plays an important role in degrading the electron mobility due to its dependence on normal electric field. As gate voltage increases, more electrons are accumulated at the surface of silicon film and surface scattering, therefore becomes the dominating mechanism limiting the electron mobility.

3 Conclusions

The present model accurately predicts the short-channel threshold voltage and drain current-voltage characteristics of SOI MOSFET over a wide range of temperature ($T > 250$ K). The analysis includes two temperature dependent empirical parameters for accurate modelling of SOI MOSFET in short-channel regime. The threshold voltage is expressed explicitly in terms of device parameters, terminal voltages and temperature. The value of $dV_{th}/dT$ is found to be of the order of - 0.83 V. The results are verified by comparing the calculated results with the experimental data available in the literature. The present model could be useful in the compact scalable model of the SOI MOSFET for circuit simulation.

Acknowledgement

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Appendix

The potential distribution in the silicon film before the onset of strong inversion is given by Poisson's Eqn:

$$\frac{d^2\Phi(x,y)}{dx^2} + \frac{d^2\Phi(x,y)}{dy^2} = \frac{qN_s(x)}{\varepsilon Si} \ldots (A-1)$$

At low drain-source voltage, the potential distribution in silicon film can be approximated by a simple parabolic function down the vertical direction

$$\Phi(x,y) = C_1(y) + xC_2(y) + x^2C_3(y) \ldots (A-2)$$

The boundary conditions on electric potential and field at front/back interface (Eq. A-3) and at source/drain (Eq. A-4) are:

$$\Phi(0,y) = \Phi_f(y), \text{ the front surface potential} \ldots (A-3(a))$$
\[
\Phi(t, y) = \Phi_n(y), \text{ the back surface potential}
\]

\[
\left[ \frac{d\Phi(x, y)}{dx} \right]_{x=0} = \frac{\varepsilon_{\text{in}}}{\varepsilon_{\text{Si}}} \left[ \Phi_f(y) - \left( V_{gs} - V_{th} \right) \right]
\]

field at front interface \hspace{1cm} ...(A-3(b))

\[
\left[ \frac{d\Phi(x, y)}{dx} \right]_{x=L} = \frac{\varepsilon_{\text{in}}}{\varepsilon_{\text{Si}}} \left[ \left( V_{ds} - V_{th} \right) - \Phi_f(y) \right]
\]

field at back interface \hspace{1cm} ...(A-3(c))

\[
\Phi_f(0) = \varphi_f, \text{ front surface potential at source}
\]

...(A-4(a))

\[
\Phi_f(L_{eff}) = \varphi_f + V_{th}, \text{ front surface potential at drain}
\]

...(A-4(b))

Substituting Eqs. (A-2), (A-3), and (A-4) in Eq. (A-4) and solving, we obtain an expression for front surface potential:

\[
\Phi_f(y) = -\sigma_f + A \exp(-y\sqrt{\alpha_f}) + B \exp(y\sqrt{\alpha_f})
\]

...(A-5)

It is assumed that the silicon film is thin enough to be fully depleted and therefore the front channel turns on before the back channel. The threshold voltage is taken to be that value of gate-source voltage for which the surface potential attains a minimum value:

\[
\Phi_f(y_{\text{min}}) = \varphi_f
\]

...(A-6)

Substituting Eq. (A-5) in Eq. (A-4), Eqns. (A-7) is obtained which leads to Eq. (6(a)).

\[
\sigma_f = \frac{C + D - \varphi_f}{1 - E}
\]

...(A-7)

References