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CMOS realization of voltage differencing gain amplifier (VDGA) and its application to biquad filter

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A circuit realization of the voltage differencing gain amplifier (VDGA) using only tunable transconductance cells is described in this paper. The newly defined element is conceptually a combination of the voltage differencing unit and the current-controlled voltage amplifier. The advantage feature of the proposed element is that the important transfer characteristics are electronically tunable by means of external bias currents. As application example, the resistorless realization of voltage-mode biquad filter based on the proposed VDGA is also introduced. PSPICE simulation results of the proposed circuit and its application are given to confirm the theoretical analysis.

Keywords: Voltage differencing gain amplifier (VDGA), Biquad filter, Resistorless realization, Voltage-mode circuit

It is well-known fact that active elements are very important in the synthesis of signal processing circuits, such as active filters, sinusoidal oscillators and immittance function simulators etc. Up to now, different kinds of high-performance active elements have been introduced[1]. One of them is voltage differencing buffered amplifier (VDBA)[2,3]. This element is introduced as an alternative to the existing current differencing buffered amplifier (CDBA)[4]. The difference between VDBA and CDBA is that the VDBA inputs are voltage as for the CDBA inputs are current. A number of analog signal processing/signal generation circuit solutions based on VDBA element have also been presented. However, the output stage of the VDBA is composed of the voltage buffer, which does not offer electronic adjustment property. Therefore, if the conventional VDBA is modified such that the voltage buffer is replaced by the tunable voltage gain amplifier, the universality of the resulting element can considerably be gained. Accordingly, let us call this element voltage differencing gain amplifier (VDGA).

In this paper, we present an alternative CMOS realization scheme of VDGA. The circuit is realized based on the employment of only tunable transconductance cells as fundamental circuits. The proposed VDGA is a simplified variant of the VDBA element by replacing the unity-gain voltage amplifier with the current-controlled voltage amplifier. This element can, therefore, be thought of as a combination of the voltage differencing unit and the voltage gain amplifier. As an application example, the resistorless realization of an electronically tunable voltage-mode biquad filter using the proposed VDGAs as active elements is also discussed. Computer simulation results with TSMC 0.35-μm *n*-well CMOS real process parameters are given to demonstrate the characteristics of the circuit and its biquad filter application, and verify the theory.

Conception of the Proposed VDGA

The schematic symbol of the proposed VDGA is shown in Fig. 1. The voltage-current characteristic of the model can be described by the following set of the circuit equations:

$$i_p = i_n = 0, \quad i_z = g_m(v_p - v_n) \text{ and}$$
$$v_w = \beta v_z \qquad \ldots (1)$$

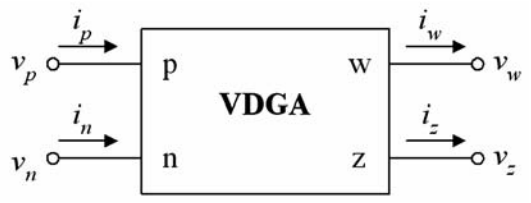

Fig 1—Circuit symbol of the VDGA

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where g_m and β denote the transconductance and voltage gain of the VDGA, respectively. It is clearly seen from Eq. (1) that the VDGA has high-impedance terminals p, n and z, and low-impedance terminal w. The difference of the v_p and v_n voltages is transformed into current i_z at the z-terminal using the transconductance g_m. The voltage v_z on this terminal is then amplified and also transferred into voltage v_w at the w-terminal by the voltage gain β. This implies that the VDGA device consists essentially of the voltage differencing unit followed by the voltage amplifier.

Realization of the Proposed VDGA

Figure 2 shows the CMOS implementation and the symbolic representation of the basic tunable transconductance cell that will be used as a fundamental circuit for realizing the proposed VDGA. The circuit is obtained from the Arbel-Goldminz transconductances[5]. For this cell, the transconductance gain (g_m) is determined by the transconductance of output transistors, which can be expressed as:

$$g_m = \frac{i_o}{v_1 - v_2} = \left(\frac{g_{m1}g_{m2}}{g_{m1}+g_{m2}}\right) + \left(\frac{g_{m3}g_{m4}}{g_{m3}+g_{m4}}\right) \quad \ldots (2)$$

where $g_{mi} = \sqrt{\mu C_{ox}(W_i/L_i)I_B}$ is the transconductance value, I_B is an external DC bias current, μ is the effective carrier mobility, C_{ox} is the gate-oxide capacitance per unit area, and W and L are the effective channel width and length of the i^{th} MOS transistor (i = 1, 2, 3, 4), respectively. It is to be noted from Eq. (2) that the value of g_m can be adjusted by bias current I_B.

Figure 3 shows the possible CMOS implementation of the proposed VDGA. It consists of only three tunable transconductance cells of Fig. 2, where the g_m-value of each cell corresponds to Eq. (2) and can be rewritten as:

$$g_{mk} = \left(\frac{g_{m1k}g_{m2k}}{g_{m1k}+g_{m2k}}\right) + \left(\frac{g_{m3k}g_{m4k}}{g_{m3k}+g_{m4k}}\right) \quad \ldots (3)$$

In Eq. (3), g_{mk} (k = A, B, C) denotes the small-signal transconductance gain of transistor M_{ik}. Also note that the value of g_{mk} can be controlled by I_{Bk}. From Fig. 3, the transconductance cell M_{1A}-M_{4A} acts as the differential-input voltage to current converter with the corresponding p, n and z terminals, i.e., $g_m = g_{mA} = i_z/(v_p - v_n)$, which is electronically controllable via I_{BA}. The pair of transconductance cells M_{1B}-M_{4B} and M_{1C}-M_{4C} is connected such that it behaves the current-controlled voltage amplifier with z and w terminals ($v_w = \beta v_z$). Its voltage gain β can be controlled electronically as the following relation:

$$\beta = \frac{v_w}{v_z} = \frac{g_{mB}}{g_{mC}} \quad \ldots (4)$$

where g_{mB} and g_{mC} are the g_m-values of the transconductance cells M_{1B}-M_{4B} and M_{1C}-M_{4C}, respectively. According to Eq. (2), the voltage gain β between v_w and v_z can be set by means of I_{BB} and I_{BC}. Note that high value of β will be obtained from moderate values of this ratio. Furthermore, with matched transconductances $g_{mnB} = g_{m1B} \cong g_{m2B}$, $g_{mpB} = g_{m3B} \cong g_{m4B}$, $g_{mnC} = g_{m1C} \cong g_{m2C}$ and $g_{mpC} = g_{m3C} \cong g_{m4C}$, the maximum β-value for the proposed VDGA given in Fig. 3 can therefore be assumed as:

$$\beta_{max} \cong \frac{(g_{mnB}+g_{mpB})_{max}}{(g_{mnC}+g_{mpC})_{min}} \quad \ldots (5)$$

The above expression reveals that the highest achievable value of β can be realized by setting the values of g_{mnB} and g_{mpB} maximum, while keeping the

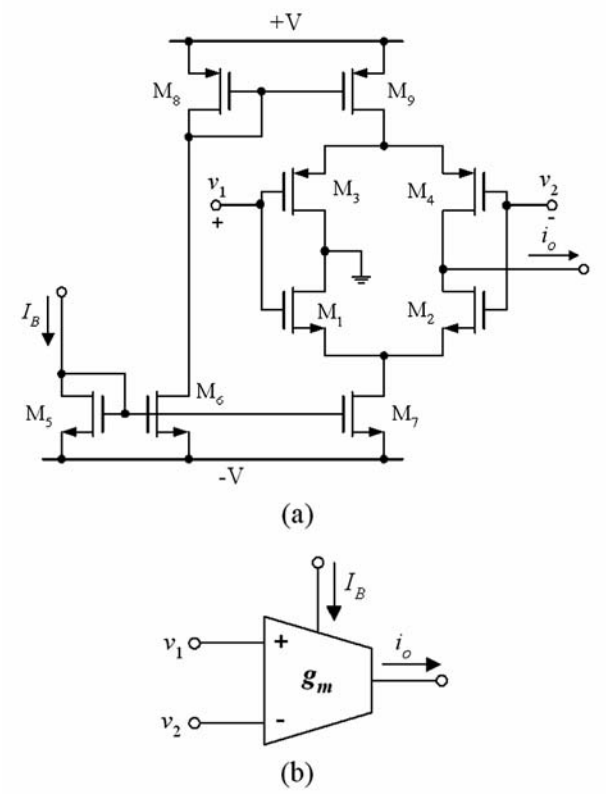

Fig 2—Tunable transconductance cell. (a) CMOS implementation (b) symbolic representation

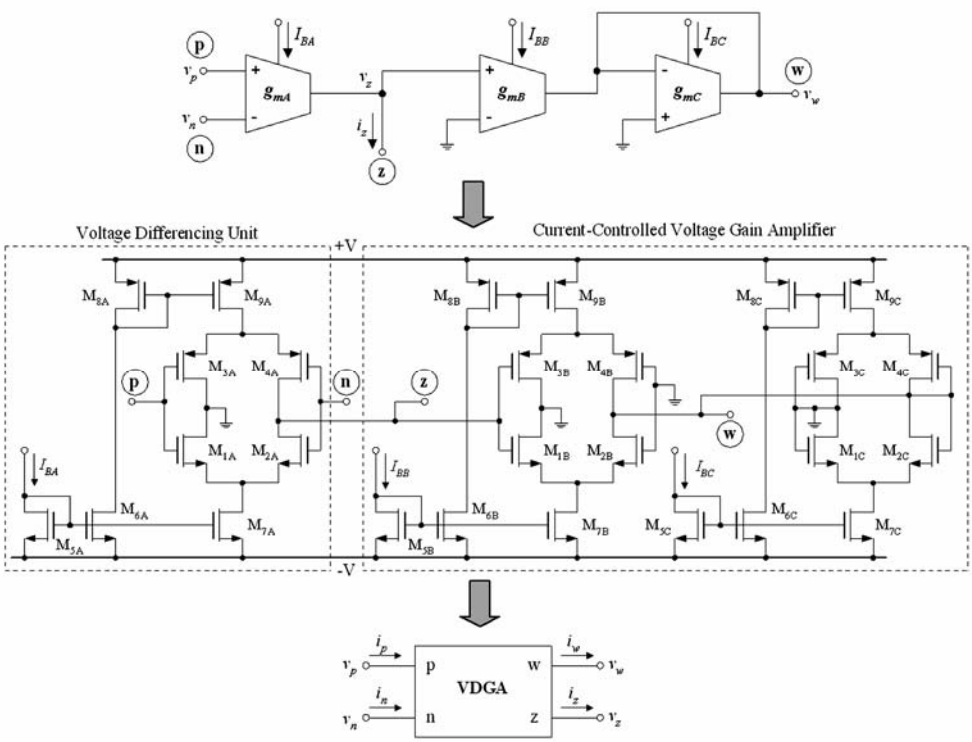

Fig 3—Possible CMOS implementation of the proposed VDGA

g_{mnC} and g_{mpC} values minimum. Consequently, it can be concluded from the above-describing relations that the defined element has the advantage feature of electronic tuning of its important parameters (g_m and β) by means of external bias currents I_{BA}, I_{BB} and I_{BC}.

The small-signal input resistance seen at terminal z is given approximately by:

$$r_z \cong \frac{(g_{m2A}+g_{o7A})(g_{m4A}+g_{o9A})}{g_{m2A}g_{o2A}(g_{m4A}+g_{o9A}) + g_{m4A}g_{o4A}(g_{m2A}+g_{o7A}) + g_{m2A}g_{m4A}(g_{o2A}+g_{o4A})} \quad \ldots (6)$$

where g_{miA} and g_{oiA} represent the transconductance value and output conductance of the transistor M_{iA}, respectively.

The output resistance at terminal w is given by :

$$r_w = \frac{g_{m1C}g_{m2C}g_{m3C}g_{m4C}}{g_{m1C}g_{m2C}(g_{m3C}+g_{m4C}) + g_{m3C}g_{m4C}(g_{m1C}+g_{m2C})} \quad \ldots (7)$$

Results and Discussion

The performance of the proposed VDGA of Fig. 3 has been simulated by PSPICE program with TSMC 0.35-µm *n*-well CMOS real process. The aspect ratios (W/L) of the transistors were selected as: M_{1k}-M_{2k} = 16.1µm/0.7µm, M_{3k}-M_{4k} = 28µm/0.7µm, M_{5k} = 7µm/0.7µm, M_{6k}-M_{7k} = 8.5µm/0.7µm, M_{8k}-M_{9k} = 21µm/0.7µm. In simulations, the supply voltages were chosen as: $+V = -V = 1.5$ V.

To demonstrate the electronic controllability of the value of g_{mk} ($k = A, B, C$), the variations of the g_{mk}-value by adjusting I_{Bk} from 0 to 200 µA are plotted in Fig. 4. The DC transfer characteristics of i_z against v_p-v_n of the proposed VDGA for various values of I_{BA} (i.e., I_{BA} = 10 µA, 20 µA, 40 µA and 80 µA) are provided by Fig. 5. This choice yields the transconductance values of the VDGA as: g_m = 190 µA/V, 270 µA/V, 380 µA/V and 540 µA/V, respectively. It can be measured from the results that the notable offset currents ($\Delta I_{BA}/I_{BA}$) were found to be: 0.22 µA, 0.47 µA, 0.95 µA and 1.78 µA, respectively. These offsets are relative difference between the currents flowing through the two braches of the transconductance cell (M_{1A}-M_{4A}) in Fig. 3. With the same setting, the frequency responses of the AC transfer characteristics of the transconductance gain (g_m) between i_z and (v_p-v_n) are also shown in Fig. 6. The 3-dB bandwidth of the input stage of the proposed VDGA in Fig. 3 is approximately found as 100 MHz.

Figure 7 depicts the simulated output voltage waveforms from the *w*-terminal (v_w) of the proposed VDGA in Fig. 3. These results are obtained for four different values of I_{BB} (i.e., I_{BB} = 10 μA, 20 μA, 40 μA, 80 μA), while I_{BC} = 10 μA and $v_z(t)$ = 10 sin ($2\pi \times 10^6$)t mV. This setting leads to obtain β = 1.0, 1.4, 2.0 and 2.8, respectively. Figure 8 shows the AC voltage transfer characteristics from *z*- to *w*-terminals ($\beta = v_w/v_z$) for the same component values given in Fig. 7. The simulated results prove that the suggested circuit can exhibit an electronically tunable voltage gain over a wide current range. Also, it can be measured that the 3-dB bandwidth in a high frequency as nearly as 100 MHz is achieved.

Application to electronically tunable biquad filter

The application example of the newly defined VDGA is demonstrated on the design of three-input single-output electronically tunable voltage-mode biquadratic filter. As shown in Fig. 9, the designed filter is constructed using only two VDGAs and two floating capacitors. Note that the floating capacitor can easily be implemented using advanced integrated circuit (IC) technologies. These new IC technologies offer a second poly layer (poly2), which also enables the realization of floating capacitors as double poly (poly1-poly2) capacitors[6]. They are standard today and are used very commonly in analog IC designs[7,8]. Thus, by employing VDGAs as active components and floating capacitors as passive components, the proposed electronically tunable voltage-mode biquadratic filter in Fig. 9 is advantageous from the integration point of view. Routine circuit analysis

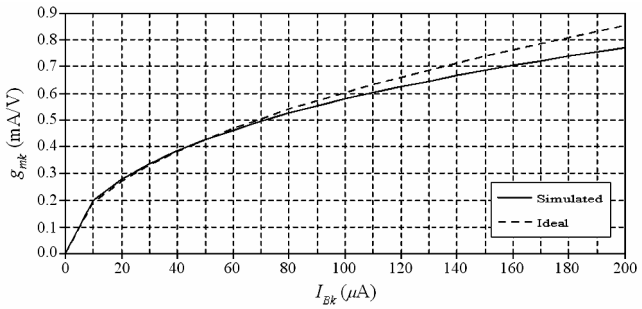

Fig 4—Variation of g_{mk}-value as a function of I_{Bk} (k = A, B, C)

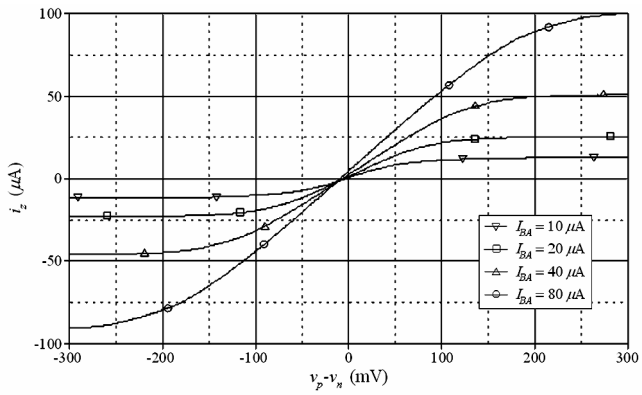

Fig 5—DC transfer characteristics between i_z and (v_p–v_n) for different values of I_{BA}

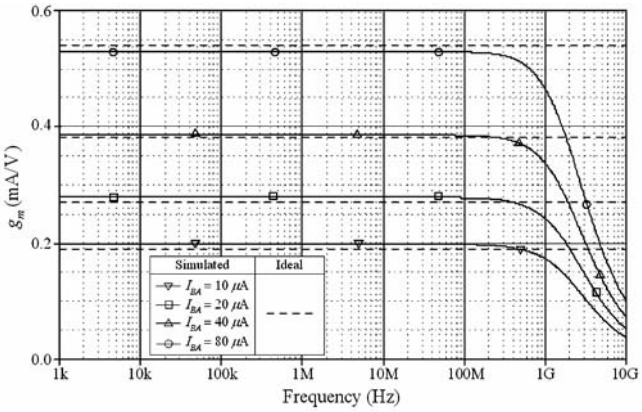

Fig 6—Frequency responses of g_m for different values of I_{BA}

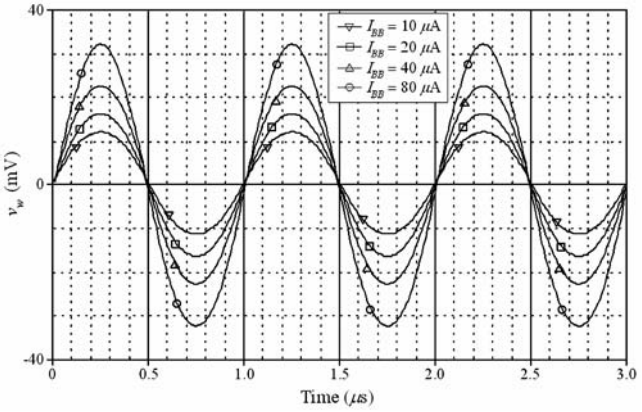

Fig 7—Time domain responses of v_w for different values of I_{BB}

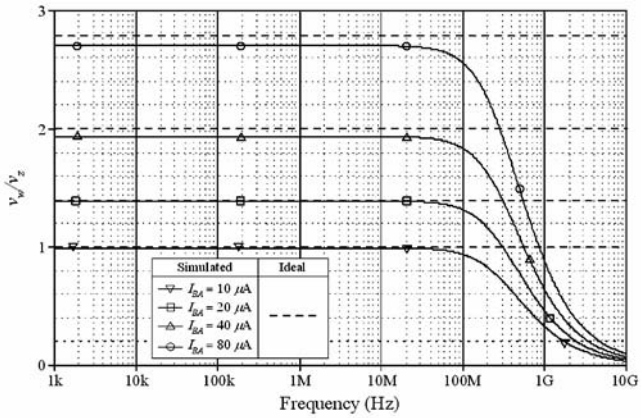

Fig.8—AC voltage transfer characteristics for different values of I_{BB}

yields the output voltage V_{out} of the circuit as the following expression:

$$V_{out} = \frac{\beta_2 s^2 V_3 + \left(\frac{\beta_1\beta_2 g_{m2}}{C_2}\right) sV_2 + \left(\frac{\beta_1\beta_2 g_{m1} g_{m2}}{C_1 C_2}\right) V_1}{s^2 + \left(\frac{\beta_2 g_{m2}}{C_2}\right) s + \left(\frac{\beta_1\beta_2 g_{m1} g_{m2}}{C_1 C_2}\right)} \quad \ldots (8)$$

where g_{mj} and β_j are the parameters g_m and β of the j^{th} VDGA (j = 1, 2). By properly selecting the relevant input voltage, the filter of Fig. 9 can realize all the five standard biquadratic filtering functions, namely lowpass (LP), bandpass (BP), highpass (HP), bandstop (BS) and allpass (AP) from the same circuit configuration, indicated as follows:

(i) If $V_1 = V_{in}$ (an input voltage signal) and $V_2 = V_3 =$ 0 (grounded), the LP response can be realized with the passband gain $H_{LP} = 1$.

(ii) If $V_2 = V_{in}$ and $V_1 = V_3 = 0$, the BP response can be realized with the passband gain $H_{BP} = \beta_1$.

(iii) If $V_3 = V_{in}$ and $V_1 = V_2 = 0$, the HP response can be realized with the passband gain $H_{HP} = \beta_2$.

(iv) If $V_1 = V_3 = V_{in}$, $V_2 = 0$ and $\beta_2 = 1$, the BS response can be realized with the passband gain $H_{BS} = 1$.

(v) If $V_1 = -V_2 = V_3 = V_{in}$ and $\beta_1 = \beta_2 = 1$, the AP response can be realized with the passband gain $H_{AP} = 1$.

It may be noted that BS and AP filter realizations require the input-signal matching conditions. In case of the inequality, if $V_1 > \beta_2 V_3$, the filter of Fig. 9 will perform a lowpass notch biquad. On the other hand, if $V_1 < \beta_2 V_3$, the filter performs a highpass notch biquad.

In all responses, the natural angular frequency (ω_0) and the quality factor (Q) for $\beta_1 = g_{mB1}/g_{mC1}$ and $\beta_2 = g_{mB2}/g_{mC2}$ can be given respectively by:

$$\omega_0 = \sqrt{\frac{g_{m1} g_{m2} g_{mB1} g_{mB2}}{g_{mC1} g_{mC2} C_1 C_2}} \quad \ldots (9)$$

and $$Q = \sqrt{\frac{g_{m1} g_{mB1} g_{mC2} C_2}{g_{m2} g_{mC1} g_{mB2} C_1}} \quad \ldots (10)$$

From Eqs (9) and (10), it can be clearly observed that the active and passive sensitivities are all halved in magnitude. Moreover, by taking $g_m = g_{m1} = g_{m2}$, $g_{mH} = g_{mB1} = g_{mC2}$, $g_{mL} = g_{mB2} = g_{mC1}$ and $C = C_1 = C_2$, Eqs (9) and (10) turn to:

$$\omega_0 = \frac{g_m}{C} \quad \ldots (11)$$

and $$Q = \frac{g_{mH}}{g_{mL}} \quad \ldots (12)$$

Note that the ω_0 can be tuned electronically by changing g_m without disturbing Q. Analogously, the Q-value can be adjusted independently by controlling the transconductance ratio g_{mH}/g_{mL}.

To verify the theoretical analyses, the circuit of Fig. 9 has been designed for $f_0 = \omega_0/2\pi \cong 3$ MHz and $Q = 1$, by taking the values of components: $I_{BAk} = I_{BBk} = I_{BCk} = 40$ μA ($g_{mk} = 380$ μA/V and $\beta_k = 1$) and $C_1 = C_2 = 20$ pF. Figure 10 presents the simulated LP, BP,

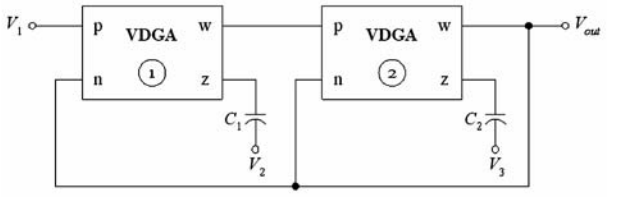

Fig 9—Electronically tunable biquadratic filter using VDGAs

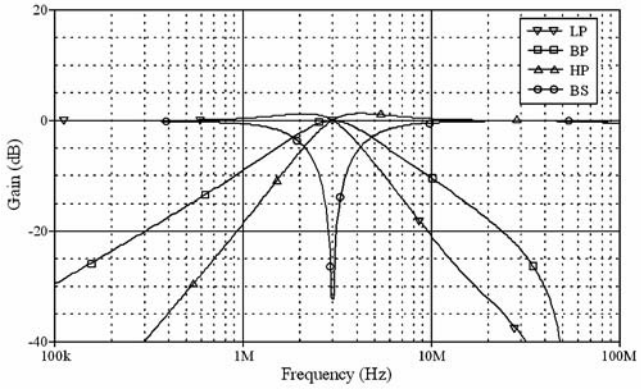

Fig 10—Amplitude-frequency responses of LP, BP, HP and BS for the designed filter of Fig.9

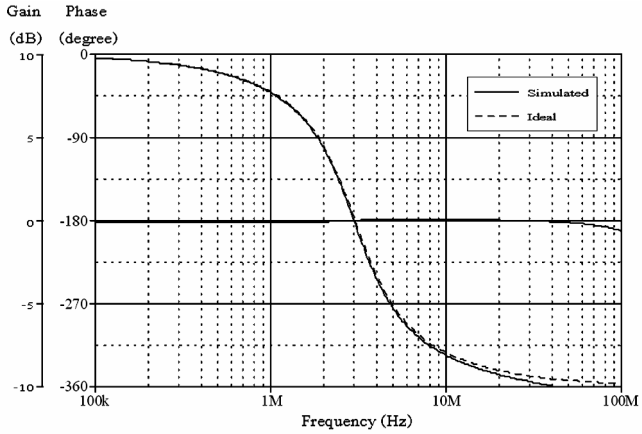

Fig 11—Amplitude and phase-frequency responses for the AP filter in Fig.9

HP and BS amplitude-frequency responses of the filter in Fig. 9. The simulated AP amplitude and phase-frequency responses are also shown in Fig. 11. The simulated f_0 is located at about 2.9 MHz. As can be seen, there is a close agreement between simulation and theory.

Figure 12 shows the simulated BP response with f_0-tuning (i.e., f_0 = 1.51 MHz, 2.15 MHz, 3.03 MHz and 4.30 MHz). In this case, the bias currents I_{BA} (= I_{BA1} = I_{BA2}) were adjusted to the values of 10 μA, 20 μA, 40 μA and 80 μA, respectively, while keeping I_{BB1} = I_{BB2} = I_{BC1} = I_{BC2} = 10 μA for Q = 1. It can be seen that the f_0 is tuned by means of I_{BA}. In Fig.13, the orthogonal controllability of the Q-value of the BP filter is demonstrated by keeping the values of I_{BA} = I_{BA1} = I_{BA2} = 40 μA (f_0 = 3.03 MHz) and I_{BB2} = I_{BC1} = 10 μA, and varying only I_{BB1} = I_{BC2} = 10 μA (Q = 1), 20 μA (Q = 1.4), 40 μA (Q = 2.0) and 80 μA (Q = 2.8), respectively. As can be observed from both figures, there are deviations occurred in the filter responses at high frequency. This is due to the fact that, in case of BP filter realization, the input signal voltage (V_{in}) is injected to the z-terminal of the VDGA1 through the floating capacitor C_1. This capacitor together with parasitic impedances at the corresponding z-terminal will introduced an extra parasitic pole. This can explain why the BP filter responses in Figs 12 and 13 have non-ideal gain responses at high frequencies. However, this effect can be reduced by choosing smaller loading capacitor.

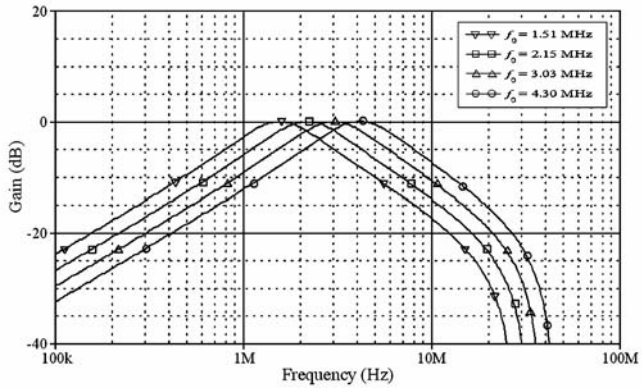

Fig 12—Amplitude-frequency responses of the BP filter when f_0 is varied

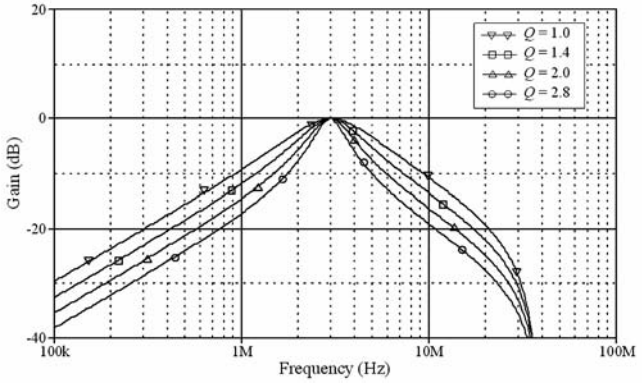

Fig 13—Amplitude-frequency responses of the BP filter when Q is varied

In addition, time domain simulation results for the BP response of the proposed filter in Fig. 9 are shown in Fig. 14, in which a 3-MHz sinusoidal input current signal with 100 mV peak value is applied to the filter. Furthermore, the total harmonic distortion (THD) variations of BP response on the amplitude of the sinusoidal input current signal at 3 MHz are plotted in Fig. 15. The results obtained indicate that the THD values of the circuit remain below 3% for sinusoidal input signals up to 100 mV peak.

In conclusion of this study, we have made a topology comparison among the previously reported multi-input single-output (MISO) voltage-mode biquads[3,9-23] and the presented biquad in Fig. 9. The summarized results are given in Table 1. From the table, it reveals that, among the topologies under comparison, the presented filter in Fig. 9 is the special one that simultaneously provides the following benefit features: resistor-free and canonical structure, simultaneous realization of all the five standard

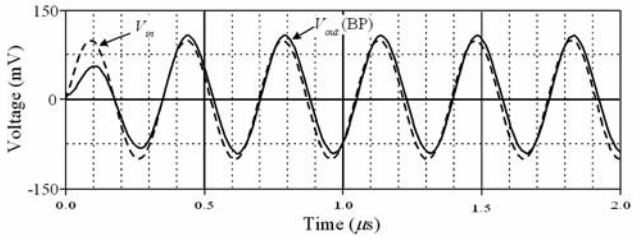

Fig 14—Time-domain response of the BP filter in Fig.9 at f_0 = 3 MHz

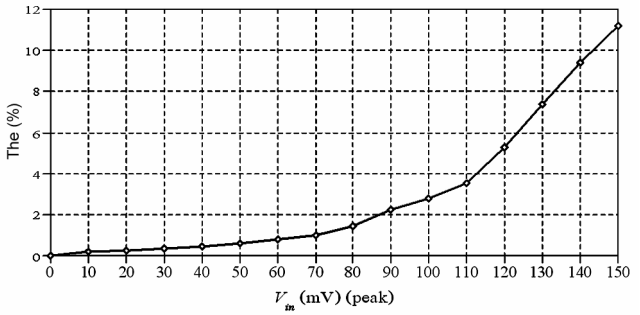

Fig 15—THD variation of the BP filter in Fig.9 at f_0 = 3 MHz

Table 1—Comparison of the proposed filter with previously available MISO-type voltage-mode biquads

Filters [Ref]	Properties							
	No. of Active components	No. of passive components	Availability of LP, BP, HP, BS and AP responses	Electronic tuning	Independent control of ω_0 and Q	Technologies	Power supplies	Power dissipation
[3]	VDBA = 2	C = 2	yes	yes	no	TSMC 0.35μm	±1.5 V	0.97 Mw
	VDBA = 2	R = 1, C = 2	yes	yes	yes			(1 VDBA)
[9]	DDCC = 2	R = 2, C = 2	yes	no	no	0.5 μm process	±3.3 V	N/A
[10]	DDCC = 3	R = 2, C = 2	yes	no	no	TSMC 0.35μm	±1.65 V	N/A
[11]	CDBA = 2	R = 4, C = 2	yes	no	no	AD844	±12 V	N/A
[12]	FDCCII = 2	R = 2, C = 2	yes	no	no	N/A	N/A	N/A
[13]	DDCC = 1,OTA = 2	C = 2	no	yes	no	TSMC 0.35μm	±1.65 V	83 mW
[14]	DDCC = 3	R = 2, C = 2	yes	no	no	TSMC 0.18μm	±1.25 V	N/A
[15]	CCCDBA = 2	C = 2	yes	yes	no	ALA400	±3 V	N/A
[16]	CFOA = 2	R = 3, C = 2	yes	no	no	AD844	±12 V	N/A
[17]	CFOA = 4	R = 5, C = 2	yes	no	yes	AD844	±5 V	N/A
[18]	DVCC = 3	R = 3, C = 2	yes	no	yes	TSMC 0.35μm	±1.5 V	3.47 mW
[19]	CCCII = 2	C = 2	yes	yes	no	AMS 0.35μm	±2.5 V	N/A
[20]	DVCC = 3	R = 4, C = 2	yes	no	no	TSMC 0.18μm	±1.25 V	4.27 mW
[21]	CFOA = 3	R = 5, C = 2	yes	no	yes	AD844	±5 V	N/A
[22]	CDBA = 1	R = 4, C = 2	yes	no	yes	AD844	±12 V	N/A
[23]	CDBA = 2	R = 4, C = 2	yes	no	yes	AD844	±12 V	N/A
Proposed	VDGA = 2	C = 2	yes	yes	yes	TSMC 0.35μm	±1.5 V	2.18 mW

DDCC : Differential difference current conveyor, DVCC : Differential voltage current conveyor, FDCCII : Fully differential current conveyor, OTA : Operational transconductance amplifier, CCCDBA : Current-controlled CDBA, CFOA : Current-feedback operational amplifier.

biquadratic filtering functions, and independent electronic tuning of ω_0 and Q.

Conclusions

A generalized active building block for analog signal processing, namely, VDGA is introduced in this work. The proposed block is implemented using only tunable transconductance cells. The VDGA-based application on the three-input single-output voltage-mode biquadratic filter realization with electronically tunable and resistor-free features has also been presented. Two VDGAs together with only two capacitors are used to realize the designed filter. It has been demonstrated that ω_0 and Q of the filter can be adjusted electronically through the parameters g_m and β of the VDGA. The feasibility of the VDGA and its application are verified by simulation results.

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