On the evaluation of Schottky barrier diode parameters of Pd, Au and Ag/n-GaAs

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Forward Voltage - Current (V-I) characteristics are generally used to investigate the Schottky barrier diode parameters, viz., barrier height, ideality factor and series resistance. This method requires a linear region (v > 3kT/q) in the ln(I) vs V characteristics. When a metal-semiconductor contact exhibits relatively high series resistance, it is difficult to determine a linear region in these forward characteristics. Therefore, one can also consider the reverse part of the V-I characteristics. Investigations are reported here on Pd, Au and Ag/n-GaAs Schottky barrier diode parameters under the whole bias range of the V-I characteristics. The theoretical and experimental results are compared and discussed.

Gallium arsenide (GaAs) is used to produce a variety of discrete and integrated optoelectronic devices, to fabricate very high speed transistors, fast computers and microwave applications, because it has a direct band gap and high electron mobility. For many years, metal-semiconductor (M-S) structure has been the subject of detailed investigations, because of its importance in advanced Very Large/Ultimate Large Scale Integrated technologies, and its fundamental interest in understanding the formation of Schottky barrier structures. The Schottky barrier structure is limited by a lack of understanding of its physical behavior and by the problem of precise determination of its parameters. However, the fundamental mechanisms of determining the physical parameters and the nature of the electrical behavior of rectifying M-S structures is still not understood satisfactorily. Several theoretical models exist, relying upon effective work functions, defects at the interface, surface state density, thermal and chemical reactivity between the metal-semiconductor contacts and inhomogeneities at the interface in order to explain the fundamental mechanism to determine the Schottky Barrier Diode (SBD) parameters. Further, under the influence of the series resistance, the V-I plot deviates from the ideal behaviour.

Recent reports on the metal-semiconductor contacts have shown that the diode parameters have been evaluated from the linear region of the forward characteristics. Aubry and Mayer have reported the limitations of the forward characteristics to determine the SBD parameters. Donoval et al. have reported a modified model which yields the barrier height of the SBD by fitting the forward characteristics, neglecting the reverse bias. A different type of external error arises when choosing the linear range from the V-I relationship plot. The series resistance influences the upper limit of the plot while various other current-transport mechanisms influence the lower bias, thus reducing the linear region. When the series resistance is large, the linear region is too small to get a reliable value of the barrier height. Furthermore, one is forced to use the region where V is small, the contribution by generation-recombination, tunneling and leakage current other than thermionic emission current will be significant in the total current. Hence, the value of saturation current is more unreliable. Investigations are reported here on the SBD parameters [barrier height (Φ_B), ideality factor (n) and series resistance (R_s)] for Pd, Au and Ag/n-GaAs from the whole bias range of the V-I characteristics.

Current Transport Mechanism

For an ideal SBD, the relationship between the current and the applied voltage from thermionic-emission theory is given by:

\[ I = I_s \left\{ \exp \left[ \frac{\beta V_D}{n} \right] - 1 \right\} \]  

where \( V_D \) is the voltage across the diode which includes series resistance (R_s), as given by \( V_D = V - IR_s \),

Therefore, Eq. (1) becomes:

\[ I = I_s \left\{ \exp \left[ \frac{\beta (V - IR_s)}{n} \right] - 1 \right\} \]  

where \( I_s = A A^* T^2 \exp (-\beta \Phi_B) \)
\( I_i \) is the saturation current, \( A \) is the area of the diode, \( A' = 8.4 \text{ Acm}^{-2} \text{K}^{-2} \) is the modified Richardson constant for GaAs, \( \phi_B \) is the barrier height, and \( \beta = \frac{\eta}{k_B T} \) is the inverse thermal voltage, where \( \eta \) is the electronic charge, \( k_B \) is the Boltzmann constant and \( T \) is the absolute temperature.

For the evaluation of the SBD parameters in both the forward and reverse bias range, one can use least square approximation condition:

\[
S = \sum_{j=1}^{N} (I_j - I_{e,j})^2 \quad \text{...(4)}
\]

where \( I_j \) is the fitting value of the current and \( I_{e,j} \) is the \( j \)th experimentally measured current. Substituting Eq.(2) in Eq.(4) and differentiating Eq.(4) w.r.t the SBD parameters, we get three normal equations [Eqs (5)-(7)]:

\[
\frac{\partial S}{\partial \phi_B} = \sum_{j=1}^{N} \frac{I_j - I_{e,j}}{[n + \beta R_s (I_j + I_e)]} \quad \text{...(5)}
\]

\[
\frac{\partial S}{\partial n} = \sum_{j=1}^{N} (I_j - I_{e,j}) \left( \frac{-\beta}{n} \right) \frac{I_j (I_j + I_e)}{[n + \beta R_s (I_j + I_e)]} \quad \text{...(6)}
\]

\[
\frac{\partial S}{\partial R_s} = \sum_{j=1}^{N} (I_j - I_{e,j}) \left( \frac{-\beta}{n} \right) \frac{I_j (I_j + I_e)}{[n + \beta R_s (I_j + I_e)]} \quad \text{...(7)}
\]

Using the three normal equations, the Pd, Au and Ag/n-GaAs SBD parameters \( \phi_B, n \) and \( R_s \) have been successfully evaluated. The theoretical and experimental \( V-I \) characteristics are compared and discussed.

Experimental

The SBDs were fabricated on LEC grown (1 0 0) silicon doped \((n = 3 \times 10^{17} \text{ cm}^{-3})\) GaAs substrates grown at Crystal Growth Centre. The substrates were polished through chemo-mechanical process. The surfaces were thoroughly cleaned in warm organic solvents (TCE, acetone and methanol) and finally etched in HCl:H\(_2\)O (1:1) solution for 60 s to remove any native oxide layer present on the surface. Schottky contacts of Pd, Au and Ag of thickness 1500 Å were deposited on the polished side of the GaAs substrate through a metallic mask. Before the metallization, Au-Ge alloy ohmic contact of thickness 2000 Å was realized on the back side of the substrate using an e-beam evaporation system followed by 5 min annealing at 703 K, under argon atmosphere. Pd, Au and Ag circular Schottky contact area of \(7.85 \times 10^{-3} \text{ cm}^2\) was used for the present investigations. The \( V-I \) characteristics of all the SBDs were measured at room temperature under dark conditions.

Results and Discussion

Fig. 1a shows the fitted \( V-I \) characteristics of the Pd/n-GaAs SBDs. The barrier height, ideality factor and series resistance of the Pd-, Au- and Ag/n-GaAs SBDs, extracted from the whole bias range, are given in Table 1. The evaluated \( \phi_B \) value of the Pd/n-GaAs SBDs is 0.87 eV while the reported value is 0.89 eV \(^9\). Furthermore, \( n \) is evaluated as 1.03. It shows that the current transport mechanism across the barrier is purely thermionic emission. The SBD parameters evaluated from the whole bias range are in agreement with the experimental results.

Figure 1b shows the experimental and simulated \( V-I \) characteristics of the Au/n-GaAs SBDs. The stimulated plot is in good agreement in the forward and reverse characteristics. The relatively lower barrier height is due to the density of the metal-semiconductor interface states and or interfacial oxide layer between metal and semiconductor. The chemical reactions between Au/GaAs were studied in detail to understand their effect on the electrical properties of the Au/GaAs system \(^9\). Cao et al. \(^11\) have proposed two models to explain the temperature dependent Schottky barrier evaluation for metal/GaAs systems. When a metal is deposited, or an oxide is formed, there is a region at the interface, which contains a mixture of micro-clusters of different phases, each having its own work function. It is known that the gold dissolves some gallium from the substrate. This produces some additional excess arsenic in the substrate to enhance the barrier height. The change in the barrier height is due to the formation of arsenic-rich region at the metal semiconductor interface. But, in our case, the lower barrier height might also be due the non-uniformity at the Au/n-GaAs interface. This has

\[
\text{Table 1} \quad \text{— The barrier height (} \phi_B \text{), ideality factor (} n \text{) and series resistance (} R_s \text{) of Pd/n-GaAs, Au/n-GaAs, and Ag/n-GaAs SBDs}
\]

<table>
<thead>
<tr>
<th>SBDs</th>
<th>Barrier height ( \phi_B ) (eV)</th>
<th>Ideality factor ( n )</th>
<th>Series resistance ( R_s ) (Ω)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Pd/n-GaAs</td>
<td>0.87</td>
<td>1.03</td>
<td>9.4</td>
</tr>
<tr>
<td>Au/n-GaAs</td>
<td>0.76</td>
<td>1.06</td>
<td>26.9</td>
</tr>
<tr>
<td>Ag/n-GaAs</td>
<td>0.82</td>
<td>1.12</td>
<td>4.8</td>
</tr>
</tbody>
</table>
mainly been attributed to the presence of native oxide that limits the ability of gold to react with the substrate. McLean et al.\textsuperscript{12} have reported that the deposition process may give rise to the presence of a greater concentration of recombination centers at the interface which produces a lowering in the "effective" barrier height and an additional path for reverse current, which is in line with our approach.

The calculated ideality factor is higher than the reported value and this is due to the contribution of the generation-recombination current through the whole bias range. The series resistance is associated with the bulk material in the semiconductor and the ohmic contact and is therefore high. One might say that this deviation accounts for the ohmic voltage drop across the bulk that adds to the junction voltage\textsuperscript{13}.

Fig. 1c shows the experimental and simulated V-I characteristics of the Ag/n-GaAs SBD. The evaluated barrier height of the diode is 0.82 eV while the reported value is 0.83 eV\textsuperscript{9}. Good agreement between theoretical and experimental values shows the validity of our approach. The observed high value of the ideality factor is due to the effect of a thick interfacial oxide layer or due to the effect of recombination in the depletion region. The departure of the ideality factor in Ag/n-GaAs far from unity is due to the inhomogeneities at the interface.

Conclusions

The barrier height values of the diodes extracted using the proposed approach match closely to the reported values determined from the experimental V-I characteristics. For the Ag/n-GaAs SBDs, the ideality factor for the whole bias is relatively high. It is attributed to the existence of a native oxide layer at the interface. The advantage of this approach is the extraction of the SBD parameters for structures with high series resistance (resistive substrates or ohmic contact with higher resistance) and there is no
necessity to have a linear part of the characteristic curve. Good agreement between the theoretical and experimental results shows validity of the approach reported here.

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References