Floating simulator with a single DVCCTA

Worapong Tangsrirat*
Faculty of Engineering, King Mongkut’s Institute of Technology Ladkrabang, Chalongkrung Road, Ladkrabang, Bangkok 10520, Thailand

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In this paper, a simple circuit configuration for simulating the floating inductor, capacitor and resistor using differential voltage current conveyor transconductance amplifier (DVCCTA) as an active element has been presented. The proposed floating simulator circuit uses only one DVCCTA and two grounded passive elements, and can realize floating inductor, capacitor or resistor depending on the passive element selection. The equivalent value of the realized simulator can be tuned electronically through the transconductance parameter of the DVCCTA. The circuit also does not require any realization conditions. The proposed circuit together with its applications is demonstrated using PSPICE simulation with 0.5 µm MIETEC CMOS technology.

Keywords: Differential voltage current conveyor transconductance amplifier (DVCCTA), Floating simulator, Inductance simulation, Capacitance multiplier

Floating simulator circuits are very useful active building blocks in many applications such as filter design, oscillator design and cancellation of parasitic elements. This is due to the well-known fact that the use of the physical inductor and capacitor, particularly of large values, is either not permitted or is unwanted in the integrated circuit technology. Accordingly, many circuits for the simulation of floating inductors and capacitors using various active elements have been introduced in the literature\(^1\)-\(^{22}\). A survey of the literature shows that the floating simulator realizations still suffer from the following weaknesses: (i) they require more than one active component\(^1\)-\(^6,8-13,15\)-\(^{20,22}\), (ii) they require at least three passive components\(^1,2,4,7,9,13-15,17,19,21\), (iii) they use some floating passive components\(^1,2,4,7,9,14,18\)-\(^{22}\) and (iv) they cannot be tuned electronically\(^1,2,4,6-9,13,14,19\)-\(^{22}\).

For example, the circuit\(^1\) proposed the floating inductance simulator by using four second-generation current conveyors (CCIIs) and three passive components, where two of them are floating. The circuits given in ref.\(^2,4\) require two dual-output CCIIs (DO-CCII), one capacitor and two resistors. The input impedance of these circuits depends on the passive components. In ref.\(^3,5\), four current-controlled current conveyors (CCCIIs) are used. The equivalent inductance value can be adjusted by changing the bias current of the CCCII. The circuits described in ref.\(^7,8,14,21\) employ a single active element and three passive elements. However, they still require one or more floating passive elements and thus, are not attractive for integration. The circuits of ref.\(^9\) need different active component types and require resistive element matching constrains for each circuit realization. The simulators described in ref.\(^10,11\) use two different types of active components; one dual-output CCCII (DO-CCCII) and one operational transconductance amplifier (OTA). Further, the other floating simulator circuits in the literature employ more than one active component\(^6,12,16,17\), or an excessive passive components\(^11,15,19,20,22\).

In this study, a simple realization of floating simulator using only one DVCCTA and two grounded passive components has been considered. The proposed floating simulator can be tuned electronically through the transconductance parameter of the DVCCTA. Since the circuit consists of only grounded passive components, it is suitable for integrated circuit implementation. Some applications together with simulation results are also given validating the performance of the proposed circuit idea.

Circuit Description

The circuit symbol and equivalent circuit of the DVCCTA are shown in Fig. 1. The differential input voltage applied across \(Y_1\) and \(Y_2\) terminals (\(v_{Y1} - v_{Y2}\))
is conveyed to voltage across the X terminal. The current applied to the X terminal is conveyed to the Z terminal. The voltage drop at the Z terminal ($v_z$) is transformed into output currents at the O+ and O- terminals with the transconductance gain ($g_m$) of the DVCCTA. Using standard notation, the terminal relations of an ideal DVCCTA shown in Fig. 1 can be characterized by the following matrix equation:

$$
\begin{bmatrix}
  i_{Y1} \\
  i_{Y2} \\
  v_X \\
  i_Z \\
  i_{O+} \\
  i_{O-}
\end{bmatrix} =
\begin{bmatrix}
  0 & 0 & 0 & 0 & 0 & 0 \\
  0 & 0 & 0 & 0 & 0 & 0 \\
  1 & -1 & 0 & 0 & 0 & 0 \\
  0 & 0 & 1 & 0 & 0 & 0 \\
  0 & 0 & 0 & g_m & 0 & 0 \\
  0 & 0 & 0 & -g_m & 0 & 0
\end{bmatrix}
\begin{bmatrix}
  v_{Y1} \\
  v_{Y2} \\
  i_X \\
  v_Z \\
  v_{O+} \\
  v_{O-}
\end{bmatrix}
$$

... (1)

The proposed floating simulator circuit consisting of one DVCCTA and two grounded passive components is shown in Fig. 2. Straightforward analysis shows that the proposed floating inductor in Fig. 2 has the following input impedance:

$$Z_{in} = \frac{Z_1}{g_m Z_2}$$  ... (2)

It is clearly seen from above expression that the circuit of Fig. 2 can simulate a floating inductor, capacitor and resistor depending on the selection of passive component as in the following choices:

(i) If $Z_1 = R_1$ and $Z_2 = 1/sC_2$ are chosen, then a lossless floating inductance simulator can be obtained as:

$$Z_{in} = \frac{sR_1 C_2}{g_m} = sL_{eq}$$  ... (3)

where the realized equivalent inductance value is found to be $L_{eq} = R_1 C_2 g_m$.

(ii) If $Z_1 = 1/sC_1$ and $Z_2 = R_2$ are chosen, then a lossless floating capacitance simulator can be obtained as:

$$Z_{in} = \frac{1}{sR_2 C_1 g_m} = \frac{1}{sC_{eq}}$$  ... (4)

where the realized equivalent capacitance value is equal to $C_{eq} = R_2 C_1 g_m$.

(iii) If $Z_1 = R_1$ and $Z_2 = R_2$ are selected, a floating resistance simulator can be realized as:

$$Z_{in} = \frac{R_1}{g_m R_2} = R_{eq}$$  ... (5)

From Eqs (3)-(5), it is obvious that the values of the $L_{eq}$, $C_{eq}$ and $R_{eq}$ can be adjusted electronically by changing the value of $g_m$ of the DVCCTA. Moreover, by setting $V_2 = 0$, a grounded impedance simulator circuit can also be realized from the proposed circuit in Fig. 2.

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Fig. 1–The DVCCTA (a) circuit symbol and (b) equivalent circuit
Fig. 2–Proposed floating simulator circuit
Non-Ideal Discussion

Effect of non-ideal gains

In practical DVCCTA device, there are non-idealities represented in voltage and current tracking errors between the Y and X terminals and the X and Z terminals, respectively. Considering these tracking errors, the actual characteristics of the DVCCTA can be represented by the following matrix equation:

\[
\begin{bmatrix}
i_Y \\
i_X \\
i_Z \\
i_{O+} \\
i_{O-}
\end{bmatrix} = \begin{bmatrix}
0 & 0 & 0 & 0 & 0 \\
0 & 0 & \beta & 0 & 0 \\
0 & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & g_m \\
0 & 0 & 0 & 0 & -g_m
\end{bmatrix} \begin{bmatrix}
v_Y \\
v_X \\
v_Z \\
v_{O+} \\
v_{O-}
\end{bmatrix}
\]

where \( \beta \) and \( \alpha \) represent the non-unity voltage and current gains, which differ from their ideally unity values by voltage and current tracking errors, respectively. Taking these non-ideal gains into consideration, the input impedance of the simulator circuit from Fig. 2 can be obtained as:

\[
Z_{in} = \frac{Z_1}{\beta \alpha g_m Z_2} \quad \text{... (7)}
\]

Equation (7) shows that non-ideal gains have affect on the input impedance value of the proposed simulator. On the other hand, the frequency dependency of these non-ideal gains should also be taken into consideration to evaluate the high-frequency performance of the circuit. Therefore, the voltage, current and transconductance gains of the DVCCTA using a single-pole model can, respectively, be defined as:

\[
\beta(s) = \frac{\beta_0}{1 + \frac{s}{\omega_\beta}} \quad \text{... (8)}
\]

\[
\alpha(s) = \frac{\alpha_0}{1 + \frac{s}{\omega_\alpha}} \quad \text{... (9)}
\]

and

\[
g_m(s) = \frac{g_{m0}}{1 + \frac{s}{\omega_p}} \quad \text{... (10)}
\]

where \( \beta_0 \), \( \alpha_0 \) and \( g_{m0} \) are the voltage, current and transconductance gains at low frequencies, and \( \omega_\beta \), \( \omega_\alpha \) and \( \omega_p \) are their corresponding pole frequencies, respectively. In general, the values of these pole frequencies will depend on practical implementation of the DVCCTA, and ideally equal to infinity. Combining Eqs (7)-(10), the operation frequency of the proposed simulator circuit in Fig. 2 can be defined as:

\[
f < (0.1/2\pi) \min{\{\alpha, \beta, \alpha_0 \}}
\]

Effect of parasitic elements

The effect of various parasitic impedances appearing at DVCCTA terminals is considered. A non-ideal equivalent circuit of the DVCCTA is shown in Fig. 3. It is shown that the practical DVCCTA has parasitic resistances \( R_y, R_z, R_x \) and parasitic capacitances \( C_y, C_z, C_x \) from \( Y_1, Y_2, Z \) and \( O \) terminals to ground, respectively, and the intrinsic resistance \( R_x \) appearing at the X terminal. If DVCCTA parasitic impedances are taken into account for the circuit in Fig. 2, the input impedances are considered as in the following:

(i) For the floating inductor \( L_{eq} \): the impedance in Eq. (3) turns to

\[
Z_{in} = \frac{R_1 + R_x}{g_m R_x} + \frac{s(R_1 + R_x)(C_2 + C_z)}{g_m} \quad \text{... (11)}
\]

Above equation indicates that there is a lossy term in the simulated impedance and thus the quality factor of the inductor is not infinite. To increase the quality factor value of the simulated inductor, a lossy term needs to be minimized. This can be achieved by choosing \( R_1 \), \( 1/g_m << R_z \) and taking large value of \( C_2 (C_2 >> C_z) \).

(ii) For the floating capacitor \( C_{eq} \): the input impedance of Eq. (4) is modified to

\[
Z_{in} = \frac{(1+sR_xC_1)(1+sR_2C_z)}{sR_2C_1g_m} \quad \text{... (12)}
\]
Eq. (9) shows that the effects of these parasitic zeros can be ignored in the frequency range of $1/R_z C_1 << \omega << 1/R_z C_2$.

(ii) For the floating resistor ($R_{eq}$): the impedance in Eq. (5) becomes

$$Z_{in} = \frac{(R_1 + R_x)(1 + sR_z C_z)}{g_m R_2}$$ \hspace{1cm} \ldots (13)

Therefore, the operating frequency of the proposed floating resistor in Fig. 2 can be defined as: $\omega << 1/R_z C_z$.

Frequency Performance Improvement

In this section, the technique to enhance the operating frequency range of the proposed simulator circuit is discussed. Considering this fact, in this study, the circuit of Fig. 2 is used for performing the inductance simulator. In practice, the non-ideal model of a floating inductance simulator can be shown in Fig. 4. It can be seen that the circuit simulates an equivalent inductor ($L_{eq}$) with additional series resistor ($R_s$) all in parallel with the resistor ($R_p$). In this model, $R_s$ limits low-frequency performance while $R_p$ restricts high-frequency performance of the simulator. Therefore, to improve the useful operating-frequency range of the circuit, unwanted parasitic resistors ($R_s$ and $R_p$) should be sufficiently reduced.

One possible method to eliminate the unwanted parasitics of the simulated inductor is to utilize the negative impedance converter (NIC)\(^2\). The electrical symbol of the NIC is shown in Fig. 5, and its terminal relations can be given by: $I_B = -I_A$ and $V_B = -V_A$. As mentioned earlier, the NIC can easily be realized from the proposed floating simulator circuit of Fig. 2 by interchanging the O+ and O- terminals of the DVCCTA. From DVCCTA-based NIC circuit of Fig. 6, the following input resistance is obtained as: $R_{AB} = -R_{eq} = -(R_1/g_{m} R_2)$. According to the equivalent non-ideal model of the proposed simulator shown in Fig. 4, the effects of $R_s$ can then be reduced by adding $R_1 = -R_s$ in series connection, as shown in Fig. 7. As a result, the low-frequency performance of the circuit is considerably improved. Similarly, to improve high-frequency performance, an additional NIC with $R_{eq} = R_p = R_p$ is also needed in parallel connection with $R_p$.

Performance Simulations

The performances of the proposed floating simulator in Fig. 2 are demonstrated by PSPICE simulation. The DVCCTA was realized by a CMOS implementation as shown in Fig. 8 using 0.5 µm MITEC CMOS technology process parameters\(^2\). The DC bias voltages were $+V = -V = 2$ V and $V_B = -1.22$ V. The aspect ratios of the MOS transistors are given in Table 1. In Fig. 8, the transconductance gain ($g_m$) of the DDCCTA can be given by:\(^2\)

$$g_m = \sqrt{kI_B}$$ \hspace{1cm} \ldots (14)

where $k = \mu C_{ox} W/L$, $\mu$ is the effective channel mobility, $C_{ox}$ is the gate-oxide capacitance per unit area, $W$ and $L$ are channel width and length, and $I_B$ is
an external DC bias current, respectively. Thus, from Eq. (14), it is possible to adjust the $g_m$-value of the DDCCTA electronically by variation of $I_B$. According to Eq. (2), it is observed that, for given values of $Z_1$ and $Z_2$, the large-value input impedance $Z_{in}$ can be realized by setting the value of $I_B$ as low as possible.

On the other hand, keeping large-value of $I_B$, small-value $Z_{in}$ can be obtained.

For the floating inductance simulation of Fig. 2, the component values used were $R_1 = 1 \, \text{k\Omega}$, $C_2 = 0.1 \, \text{nF}$ and $g_m \equiv 0.25 \, \text{mA/V}$ ($I_B \equiv 100 \, \mu\text{A}$), which results in $L_{eq} = 0.4 \, \text{mH}$. The simulated voltage and current waveforms of the proposed floating inductance simulator circuit of Fig. 2 when a 1-MHz sinusoidal signal is applied are shown in Fig. 9. From the results, it can be measured that the phase shift between the current and voltage is 85°, which is in close correspondence with the expected value equal to 90°. The impedance of the simulator versus frequency is shown in Fig. 10. It can be observed that the simulator operates correctly along the frequency range 30 kHz to 30 MHz. In Fig. 11, the frequency characteristics of the inductance simulator for various $g_m$ values are also shown. The simulations were performed by

### Table 1—Transistor aspect ratios for the DVCCTA circuit shown in Fig. 8

<table>
<thead>
<tr>
<th>Transistors</th>
<th>$W$ ($\mu\text{m}$)</th>
<th>$L$ ($\mu\text{m}$)</th>
</tr>
</thead>
<tbody>
<tr>
<td>$M_1 - M_4$</td>
<td>1.8</td>
<td>0.7</td>
</tr>
<tr>
<td>$M_5 - M_6$</td>
<td>5.2</td>
<td>0.7</td>
</tr>
<tr>
<td>$M_7 - M_8$</td>
<td>20</td>
<td>0.7</td>
</tr>
<tr>
<td>$M_9 - M_{10}$</td>
<td>17</td>
<td>0.7</td>
</tr>
<tr>
<td>$M_{11} - M_{12}$</td>
<td>58.1</td>
<td>0.7</td>
</tr>
<tr>
<td>$M_{13} - M_{14}$</td>
<td>4</td>
<td>1.0</td>
</tr>
<tr>
<td>$M_{15}, M_{18}, M_{21} - M_{24}$</td>
<td>4.5</td>
<td>1.0</td>
</tr>
<tr>
<td>$M_{16}, M_{17}, M_{19} - M_{20}$</td>
<td>5.2</td>
<td>1.0</td>
</tr>
</tbody>
</table>

![Fig. 8–CMOS implementation of the DVCCTA](image)

![Fig. 9–Waveforms of voltage and current for the floating inductance simulator of Fig. 2](image)
varying $g_m \approx 0.25 \text{ mA/V}$ ($I_B = 100 \mu A$), $0.35 \text{ mA/V}$ ($I_B = 200 \mu A$) and $0.44 \text{ mA/V}$ ($I_B = 300 \mu A$) to obtain $L_{eq} = 0.40 \text{ mH}$, $0.28 \text{ mH}$ and $0.22 \text{ mH}$, respectively.

Likewise, for the floating capacitance simulator of Fig. 2, it is realized with the following component values : $C_1 = 0.1 \text{ nF}$, $R_2 = 1 \text{ k}\Omega$ and $g_m \approx 0.25 \text{ mA/V}$, to obtain $C_{eq} = 25 \text{ pF}$. The time-domain signal waveforms are shown in Fig.12, which demonstrates that the circuit performs the capacitance behavior as expected. The impedance of the simulator circuit relative to frequency is shown in Fig.13, and the plots of impedance values with different $g_m$ are also shown in Fig.14. It appears that the simulated capacitance can be adjusted by tuning $g_m$ of the DVCCTA. To conclude, total power dissipation of the floating simulator circuit presented in Fig. 2 when $I_B = 100 \mu A$ is approximately equal to 3 mW.

**Application Examples**

As an example to demonstrate an application of the proposed floating inductor of Fig. 2, it is employed in the RLC bandpass filter as shown in Fig. 15. The floating inductor circuit is simulated with the following component values: $R_1 = 1 \text{ k}\Omega$, $C_2 = 0.1 \text{ nF}$
and \( g_m \cong 0.25 \text{ mA/V} \) \( (I_B = 100 \text{ } \mu \text{A}) \), which results in \( L_{eq} = 0.4 \text{ mH} \). Figure 16 shows the frequency responses of the bandpass filter of Fig. 15, which appears that the ideal and simulated magnitude and phase responses are in good agreement for a set of selected values over several decades.

Furthermore, to verify the performance of the derived capacitance simulator of Fig. 2, the resistively terminated LC highpass filter shown in Fig. 17 filter was designed and simulated. This filter was designed to realize third-order highpass Butterworth characteristic with the de-normalized cut-off frequency of \( f_c = \omega_c/2\pi = 3.18 \text{ MHz} \). The circuit was simulated with the ideal capacitor and our proposed floating capacitor. For this purpose, the following component values were taken for the floating capacitance simulators in Fig. 2: \( C_1 = 0.1 \text{ nF} \), \( R_2 = 1 \text{ k}\Omega \) and \( g_m \cong 0.25 \text{ mA/V} \). The theoretical and simulation results for the filter of Fig. 17 are given in Fig. 18.

In order to verify the feasibility of the proposed grounded inductance simulator of Fig. 2 and to demonstrate its application, the RLC parallel resonance circuit is designed as shown in Fig. 19. The DVCCTA circuit components are selected as: \( R_1 = 1 \text{ k}\Omega \) and \( C_2 = 0.1 \text{ nF} \). Figure 20 shows the frequency characteristics of the \( Z_{in} \) of the parallel resonance circuit in Fig. 19 for three different values of \( I_B \). From Fig. 20, we can see that the resonance frequency can be tuned electronically by the biasing.
current $I_B$ of the proposed grounded inductor, thereby verifying the proper operation and providing the flexibility of the presented circuit.

Conclusions

In this article, the floating simulator circuit using a single DVCCTA and two grounded passive components is presented. The values of the simulated inductance, capacitance and resistance can be controlled electronically by the $g_m$-value of the DVCCTA. The operation of the proposed circuit is validated on the second-order bandpass and third-order Butterworth highpass filters. All simulation results obtained through PSPICE with 0.5-µm MIETEC CMOS technology verify the workability performance of the proposed floating simulator circuit.

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References