High input impedance DDCC-based voltage-mode universal biquadratic filter with three inputs and five outputs

Jiun-Wei Horng* & Wei-Yuan Chiu
Department of Electronic Engineering, Chung Yuan Christian University, Chung-Li, 32023, Taiwan

Received 29 October 2010; accepted 20 May 2011

A new versatile high input impedance voltage-mode universal biquadratic filter with three inputs and five outputs is presented. The proposed circuit uses three plus-type differential difference current conveyors (DDCCs), two grounded capacitors and two resistors. The circuit offers realizing all the standard filter functions, that is, highpass, bandpass, lowpass, notch, and allpass filters, simultaneously, without component matching conditions, using grounded capacitors, high input impedance and low active and passive sensitivities.

Keywords: Universal biquad, Current conveyor, Active filter

The applications and advantages in the realization of various active transfer functions using current conveyors have received considerable attention. Voltage-mode active filters with high input impedance are of great interest because several cells of this kind can be directly connected in cascade to implement higher-order filters. Recently, many voltage-mode biquadratic filters with multi-inputs were presented. From the multi-inputs biquadratic circuits, all standard filter functions can be obtained in the same circuit by choosing appropriate input voltage nodes. However, only two filter functions at most can be obtained in each circuit realization.

To obtain various filter functions simultaneously in the same circuit topology will increase the usability and reduce the cost of the circuit. Therefore, several circuits with one-input and multi-outputs were presented. However, the circuits reported elsewhere can obtain three standard filter functions simultaneously only. In 1998, Abuelma’atti and Al-Zaher proposed a filter circuit configuration with one-input and five-outputs using five current feedback amplifiers (CFAs), two grounded capacitors and six resistors. All standard filter functions (lowpass, bandpass, highpass, notch and allpass) can be obtained simultaneously in the same circuit configuration. Thereafter several circuit configurations with one input and five outputs are presented. Horng et al. proposed six circuit configurations with one-input and five-outputs. Each of the first two circuits reported earlier employs four second-generation current conveyors (CCIs), two grounded capacitors and five resistors. The third circuit employs two CCIs, one differential voltage current conveyor (DVCC) and five capacitors and five resistors. The fourth circuit employs two MOCCIs, two grounded capacitors and five resistors. The circuit employs three DVCCs, two grounded capacitors and four resistors. The circuit employs two DVCCs, two grounded capacitors and three resistors. Chen, Minaei and Yuce also proposed several one-input and five-outputs universal biquads. Each of these circuits uses two (or three) current conveyors, three resistors and two capacitors. However, these circuits employ extra passive components and require component matching conditions in the realizations of allpass filter functions.

Circuit design using the differential difference current conveyors (DDCC) or DVCC as active elements received considerable attention due to the advantages of higher signal bandwidth, wider dynamic range, greater linearity and the ability of handling differential signals. Therefore, many filter circuits were presented by using DDCCs or DVCCs.

In this paper, a new versatile high input impedance voltage-mode universal biquadratic filter with three inputs and five outputs is presented. The proposed
circuit employs three plus-type DDCCs, two grounded capacitors and two resistors. The proposed circuit can realize all the standard filter functions: lowpass, bandpass, highpass, notch and allpass, simultaneously. Moreover, the proposed circuit has the following features: uses only grounded capacitors; needs not critical component matching condition and high input impedance. Since the implementation of the plus-type DDCC is simpler than that of the minus-type DDCC, the proposed circuit employs the plus-type DDCCs only. The proposed circuit uses less passive components and needs not component matching condition with respect to the previous one-input and five-outputs universal biquadratic filters.

Proposed Circuit

Using standard notation, the port relations of an ideal DDCC can be characterized by the following matrix equation:

\[
\begin{bmatrix}
V_x \\
I_{y1} \\
I_{y2} \\
I_{y3} \\
I_
u
\end{bmatrix}
= 
\begin{bmatrix}
1 & -1 & 1 & 0 & & & & & \\
0 & 0 & 0 & 0 & & & & & \\
0 & 0 & 0 & 0 & & & & & \\
0 & 0 & 0 & 0 & & & & & \\
0 & 0 & 0 & 0 & & & & & \\
\end{bmatrix}
\begin{bmatrix}
V_{y1} \\
V_{y2} \\
V_{y3} \\
I_x
\end{bmatrix}
\]

where the plus and minus signs indicate whether the conveyor is configured as a non-inverting or inverting circuit, termed DDCC+ or DDCC−.

The proposed configuration is shown in Fig. 1. Using nodal analysis, the input-output relationship matrix form can be expressed as:

\[
\begin{bmatrix}
sC_1 & -G_2 & 0 & 0 & 0 \\
G_1 & sC_2 + G_1 & 0 & 0 & 0 \\
0 & 1 & 1 & 0 & 0 \\
0 & 2 & 0 & 1 & 0 \\
1 & 1 & 0 & 0 & 1
\end{bmatrix}
\begin{bmatrix}
V_{out1} \\
V_{out2} \\
V_{out3} \\
V_{out4} \\
V_{out5}
\end{bmatrix}
= 
\begin{bmatrix}
-G_2V_{in3} \\
G_1V_{in1} + G_1V_{in2} \\
V_{in1} \\
V_{in1} + V_{in3} \\
V_{in1} + V_{in2}
\end{bmatrix}
\]

From the above matrix form, the output voltages can be obtained as:

\[(3) \quad V_{out1} = \frac{G_1G_2V_{in1} + G_1G_2V_{in2} - (sC_2G_2 + G_1G_2)V_{in3}}{s^2C_1C_2 + sC_1G_1 + G_1G_2} \]

\[(4) \quad V_{out2} = \frac{sC_1G_1V_{in1} + sC_1G_1V_{in2} + G_1G_2V_{in3}}{s^2C_1C_2 + sC_1G_1 + G_1G_2} \]

\[(5) \quad V_{out3} = \frac{(s^2C_1C_2 + G_1G_2)V_{in1} - sC_1G_1V_{in2} - G_1G_2V_{in3}}{s^2C_1C_2 + sC_1G_1 + G_1G_2} \]

\[(6) \quad V_{out4} = \frac{(s^2C_1C_2 - sC_1G_1 + G_1G_2)V_{in1} - 2sC_1G_1V_{in2}}{s^2C_1C_2 + sC_1G_1 + G_1G_2} \]

Fig. 1—The proposed universal filter.
\[ V_{out5} = \frac{s^2 C_1 C_2 V_{in1} + s^2 C_1 C_2 V_{in2} + s C_2 G_2 V_{in3}}{s^2 C_1 C_2 + s C_1 G_1 + G_1 G_2} \]  
\[ \ldots (7) \]

From Eqs (3)-(7), we can see that six circuit types can be obtained from Fig. 1:

(i) If \( V_{in2} = V_{in3} = 0 \) (grounded), then \( V_{in1} = \) input voltage signal, a bandpass filter can be obtained at \( V_{out1} \), a lowpass filter can be obtained at \( V_{out2} \), a notch filter can be obtained at \( V_{out3} \), an allpass filter can be obtained from \( V_{out4} \) and a highpass filter can be obtained from \( V_{out5} \).

(ii) If \( V_{in1} = V_{in3} = 0 \) (grounded), then \( V_{in2} = \) input voltage signal, a lowpass filter can be obtained at \( V_{out1} \), three bandpass filters can be obtained at \( V_{out2} \) or \( V_{out3} \) or \( V_{out4} \) and a highpass filter can be obtained from \( V_{out5} \).

(iii) If \( V_{in1} = V_{in2} = 0 \) (grounded), then \( V_{in3} = \) input voltage signal, two lowpass filters can be obtained at \( V_{out2} \) or \( V_{out3} \) and a bandpass filter can be obtained from \( V_{out5} \).

(iv) If \( V_{in1} = 0 \) (grounded), then \( V_{in2} = V_{in3} = \) input voltage signal, a bandpass filter can be obtained at \( V_{out1} \).

(v) If \( V_{in2} = 0 \) (grounded), then \( V_{in1} = V_{in3} = \) input voltage signal, a bandpass filter can be obtained at \( V_{out1} \) and two highpass filters can be obtained at \( V_{out3} \) and \( V_{out4} \).

(vi) If \( V_{in3} = 0 \) (grounded) and \( V_{in1} = V_{in2} = \) input voltage signal, a lowpass filter can be obtained at \( V_{out1} \), a bandpass filter can be obtained at \( V_{out2} \), an allpass filter can be obtained from \( V_{out3} \) and a highpass filter can be obtained from \( V_{out5} \).

The resonance angular frequency \( \omega_o \) and the quality factor \( Q \) are given by

\[ \omega_o = \sqrt{\frac{G_1 G_2}{C_1 C_2}} \]  
\[ \ldots (8) \]

And

\[ Q = \sqrt{\frac{C_2 G_2}{C_1 G_1}} \]  
\[ \ldots (9) \]

From circuit type 1, the proposed filter is capable of realizing all filter functions, that is, highpass, bandpass, lowpass, notch, and allpass filters simultaneously in the same configuration without component matching conditions. Due to the three input signals, \( V_{in1} \), \( V_{in2} \), and \( V_{in3} \) are connected directly to the high input impedance input nodes of the three DDCCs (the \( y \) port of the DDCC), respectively, the circuit enjoys the feature of high input impedance. The proposed circuit uses only two grounded capacitors, which are attractive for integrated circuit implementation.

**Sensitivities Analysis**

Taking the non-idealities of the DDCC into account, the relationship of the terminal voltages and currents can be rewritten as:

\[
\begin{bmatrix}
V_x \\
I_{y1} \\
I_{y2} \\
I_{y3} \\
I_z
\end{bmatrix} =
\begin{bmatrix}
\alpha_{k1}(s) & -\alpha_{k2}(s) & \alpha_{k3}(s) & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & \pm\beta_k(s) & 0 & 0 & 0 & 0 & 0 \\
\end{bmatrix}
\]
\[ \ldots (10) \]

where \( \alpha_{k1}(s) \), \( \alpha_{k2}(s) \), and \( \alpha_{k3}(s) \) represent the frequency transfer functions of the internal voltage followers and \( \beta_k(s) \) represent the frequency transfer function of the internal current follower of the \( k \)-th DDCC. They can be approximated by first order lowpass functions, which can be considered to have a unity value for frequencies much lower than their corner frequencies. If the circuit is working at frequencies much lower than the corner frequencies, then \( \alpha_{k1}(s) \approx 1 - \varepsilon_{k1} \) and \( \varepsilon_{k1} = \frac{1}{\alpha_{k1}} \approx 1 \) denotes the voltage tracking error from \( y_1 \) terminal to \( x \) terminal of the \( k \)-th DDCC, \( \alpha_{k2}(s) = 1 - \varepsilon_{k2} \) and \( \varepsilon_{k2} = \frac{1}{\alpha_{k2}} \approx 1 \) denotes the voltage tracking error from \( y_2 \) terminal to \( x \) terminal of the \( k \)-th DDCC, \( \alpha_{k3}(s) = 1 - \varepsilon_{k3} \) and \( \varepsilon_{k3} = \frac{1}{\alpha_{k3}} \approx 1 \) denotes the voltage tracking error from \( y_j \) terminal to \( x \) terminal of the \( k \)-th DDCC and \( \beta_k(s) \approx \beta_k = \)}
\( 1 - \varepsilon_{ki} \) and \( \varepsilon_{ki} \) \( (\varepsilon_{ki} << 1) \) denotes the current tracking error of the \( k \)-th DDCC. The denominator of the non-ideal voltage transfer function in Fig. 1 becomes

\[
D(s) = s^2 C_1 C_2 + s C_1 G_1 a_{12} a_{21} \beta_2 + G_1 G_2 a_{22} \beta_1 \beta_2 (a_{12} a_{31} - a_{12} + a_{32}) \quad \ldots \quad (11)
\]

The resonance angular frequency \( \omega_o \) and quality factor \( Q \) are obtained by

\[
\omega_o = \sqrt{\frac{G_1 G_2 a_{22} \beta_1 \beta_2 (a_{12} a_{31} - a_{12} + a_{32})}{C_1 C_2}} \quad \ldots \quad (12)
\]

And

\[
Q = \frac{1}{a_{12} a_{32}} \sqrt{\frac{C_2 G_2 a_{22} \beta_1 (a_{12} a_{31} - a_{12} + a_{32})}{C_1 G_1 \beta_2}} \quad \ldots \quad (13)
\]

The active and passive sensitivities of \( \omega_o \) and \( Q \) are shown as

\[
S^{\omega_o}_{G_1, G_2} = -S^{\omega_o}_{a_{12}, a_{32}} = \frac{1}{2} \quad S^{\omega_o}_{a_{22}, \beta_2} = \frac{1}{2} \quad S^{\omega_o}_{a_{31}, a_{32}} = \frac{1}{2} \quad S^{\omega_o}_{a_{12}, \beta_1} = 0
\]

\[
S^Q_{a_{12}} = -S^Q_{\beta_2} = \frac{1}{2} \quad S^Q_{a_{21}} = 1 \quad S^Q_{a_{31}} = -1
\]

The sensitivity values were calculated by assuming that \( \alpha \) and \( \beta \) are near to unity. All the active and passive sensitivities are small.

**Influence of Parasitic Elements**

A non-ideal DDCC model is shown in Fig. 2\(^19\). It is shown that the real DDCC has parasitic resistors and capacitors from the \( y_1, y_2, y_3 \) and \( z \) terminals to the ground, and also, a series resistor at the input terminal \( x \). Taking into account the non-ideal DDCCs and assuming the circuits are working at frequencies much lower than the corner frequencies of \( \alpha_i(s) \) and \( \beta_j(s) \), namely, \( \alpha_i \equiv \beta_j \equiv 1 \).

Moreover, in practical DDCCs, the external resistors can be chosen to be much smaller than the parasitic resistors at the \( y \) and \( z \) terminals of DDCCs and much greater than the parasitic resistors at the \( x \) terminals of DDCCs, i.e., \( R_y, R_z \gg R_k \gg R_x \). The external capacitances \( C_1 \) and \( C_2 \) can be chosen to be much greater than the parasitic capacitors at the \( y \) and \( z \) terminals of DDCCs, i.e., \( C_y, C_z \ll C_1, C_2 \). Under these conditions, the output voltages of Fig. 1 become

\[
V_{out1} \equiv \frac{(s^2 C_1 G_1 G_2 x_1 + s C_1 G_2 G_1 x_2 + G_1 G_2 G_1 W_{in1} + (-s C_1 G_1 G_2 G_1 W_{in2} + (s C_2 G_1 G_2 G_1 W_{in3}) x_1 + s C_1 G_1 G_2 G_1 x_2 G_2 G_1)}{s^3 C_1 G_1 G_2}} \quad \ldots \quad (14)
\]

![Fig. 2—The non-ideal DDCC model](image-url)
\[
(V_{in1} + sC' G' G_{x1} + (s^2 G' G_{x1}) V_{in2}) \frac{V_{out2}}{s^3 C' C' C_x + s^2 C' C' G_{x1} + sC' G_{x1} G_{x1} + G_{x1} G_{x1} G_{x1}} \text{ ... (15)}
\]

\[
V_{out3} \equiv \frac{(s^2 C' C' G_{x1} + sC' G_{x1} G_{x1} + G' G_{x1}) V_{in2}}{s^3 C' C' C_x + s^2 C' C' G_{x1} + sC' G_{x1} G_{x1} + G_{x1} G_{x1} G_{x1}} \text{ ... (16)}
\]

\[
V_{out4} \equiv \frac{(s^2 C' C' G_{x1} + sC' G_{x1} G_{x1} + G' G_{x1}) V_{in2}}{s^3 C' C' C_x + s^2 C' C' G_{x1} + sC' G_{x1} G_{x1} + G_{x1} G_{x1} G_{x1}} \text{ ... (17)}
\]

\[
V_{out5} \equiv \frac{(s^2 C' C' G_{x1} + sC' G_{x1} G_{x1} + G' G_{x1}) V_{in2}}{s^3 C' C' C_x + s^2 C' C' G_{x1} + sC' G_{x1} G_{x1} + G_{x1} G_{x1} G_{x1}} \text{ ... (18)}
\]

Where

\[ C' = C_1 + C_{y1} + C_{y2}, C' = C_2 + C_{y3} + C_{y2}, \]

\[ C_3 = C_{y21} + C_{y31}, R' = R_1 + R_{x3}, R'' = R_2 + R_{x2}, \]

\[ G_3 = G_{y1} + G_{y32}, G_4 = G_{y21} + G_{y2} + G_{y22} \]

and

\[ G_5 = G_{y21} + G_{y31}. \]

In Eqs (14)-(18), undesirable factors are yielded by the non-idealities of the DDCCs. To minimize the effects of the DDCCs' non-idealities, the operation angular frequency should restricted to the following conditions:

\[
\omega << \min \left\{ \frac{1}{C_2 C_3 R' R_2}, \frac{1}{C_2 R_2}, \sqrt{1 \over \frac{C'_1 R_x}{C'_1 C'_2 R'_1 R_1}}, \frac{R_4}{(C'_1 R_3 + C'_2 R_4) R'_1 R_1} \right\} \text{ ... (19)}
\]

\[
\omega >> \max \left\{ \frac{|R_3 - R_4|}{C'_1 R_x R_5}, \frac{1}{C'_1 R_3}, \frac{C_1 R_5 + C'_2 R_4 R_5 - C'_2 R_4 R'_1}{C'_1 C'_2 R'_1}, \frac{1}{\sqrt{C'_1 C'_2 R'_1 R_3}} \right\} \text{ ... (20)}
\]

Moreover, application of the Routh-Hurwitz test to the denominator of Eq. (14) shows that \( C_3 \) may cause the root with positive real part. According to this test, the roots of the denominator will keep in left-half s-plane if

\[ C'_1 R'_1 > C_1 R_x \] ... (21)

It is not difficult to satisfy this condition, since the external capacitance \( C_1 \) and resistance \( R_2 \) can be chosen much greater than \( C_3 \) and \( R_x \), respectively.

**Simulation Results**

HSPICE simulations were carried out to demonstrate the feasibility of the proposed circuit in Fig. 1. The DDCC was realized by the CMOS implementation in Fig. 3. The simulations use

Fig. 3—The CMOS realization of the plus-type DDCC.
0.18 µm, level 49 CMOS technology process parameters from TSMC (Taiwan Semiconductor Manufacturing Company, Ltd.) and the aspect ratios of the MOS transistors were chosen in Table 1. The supply voltages are $V_{dd} = +1.25$ V, $V_{ss} = -1.25$ V and $V_b = -0.68$ V. Figures 4 (a), (b), (c), (d) and (e) represent the simulated frequency responses for the

![Fig. 4—Simulation results of the proposed universal filter (a) Lowpass filter ($V_{out1}$), (b) Bandpass filter ($V_{out2}$), (c) Notch filter ($V_{out3}$), (d) Allpass filter ($V_{out4}$), (e) Highpass filter ($V_{out5}$), designed with $V_{in1}$ = input voltage signal and $V_{in2} = V_{in3} = 0$ (grounded)]
lowpass ($V_{out1}$), bandpass ($V_{out2}$), notch ($V_{out3}$), allpass ($V_{out4}$), and highpass ($V_{out5}$) filters of Fig. 1, respectively, designed with $V_{in1} =$ input voltage signal, $V_{in2} = V_{in3} = 0$ (grounded), $Q = 1$ and $f_o = 15.915$ MHz: $C_1 = C_2 = 10$ pF and $R_1 = R_2 = 1$ kΩ. The DDCC has parasitic resistor from the $z$ terminal to the ground ($R_z$). When the $z$ terminal load of the DDCC is a capacitor ($C$), it introduces a pole produced by $R_z$ and $C$ at low frequency. This can explain why Figs 4(b) and 4(e) have non-ideal phase responses at low frequencies. This effect can be minimized by using larger loading capacitors or operating the filters in high frequencies.

Figure 5 represents the simulated gain responses for the bandpass filter, designed with $V_{in1} =$ input voltage signal, $V_{in2} = V_{in3} = 0$ (grounded), $V_{out2} =$ output voltage signal, $Q = 2$ and $f_o = 15.915$ MHz: $C_1 = C_2 = 10$ pF and $R_1 = R_2 = 1$ kΩ.

Figure 6 represents the simulated frequency responses for the allpass filter of Fig. 1, designed with $V_{in1} = V_{in2} =$ input voltage signal, $V_{in3} =$ output voltage signal, $Q =$ and $f_o = 15.915$ MHz: $C_1 = C_2 = 10$ pF and $R_1 = R_2 = 1$ kΩ.

Fig. 5—Simulated gain responses for the bandpass filter ($V_{out2}$), designed with $V_{in1} =$ input voltage signal, $V_{in2} = V_{in3} = 0$ (grounded) and $Q = 2$.

Fig. 6—Simulated frequency responses for the allpass filter ($V_{out4}$), designed with $V_{in1} = V_{in2} =$ input voltage signal and $V_{in3} = 0$ (grounded)

Fig. 7—Simulated gain responses for the bandpass filter ($V_{out3}$), designed with $V_{in2} =$ input voltage signal, $V_{in1} = V_{in3} = 0$ (grounded) and $Q = 4$.

Fig. 8—(a) Time-domain input (upper signal) and output signal waveforms to demonstrate the ac dynamic range of the proposed filter, designed with $V_{in1} =$ input voltage signal, $V_{in2} = V_{in3} = 0$ (grounded) and $V_{out2} =$ output voltage signal and (b) Time-domain input (upper signal) and output signal waveforms to demonstrate the ac dynamic range of the proposed filter, designed with $V_{in2} =$ input voltage signal, $V_{in1} = V_{in3} = 0$ (grounded) and $V_{out1} =$ output voltage signal.
Figure 7 represents the simulated gain responses for the bandpass filter of Fig. 1, designed with $V_{in2} =$ input voltage signal, $V_{in1} = V_{in3} = 0$ (grounded), $V_{out3} =$ output voltage signal, $Q = 4$ and $f_o = 15.915$ MHz: $C_1 = C_2 = 10$ pF and $R_1 = 4$ k$\Omega$, $R_2 = 0.25$ k$\Omega$.

Figure 8a shows the input and output signals of bandpass response of the proposed filter designed with $V_{in1} =$ input voltage signal, $V_{in2} = V_{in3} = 0$ (grounded), $V_{out2} =$ output voltage signal and $Q = 1$: $C_1 = C_2 = 10$ pF and $R_1 = R_2 = 1$ k$\Omega$. It is observed that 15.9 MHz with 170 mVp-p input voltage signal levels are possible without significant distortion.

Figure 8b shows the input and output signals of bandpass response of the proposed filter designed with $V_{in2} =$ input voltage signal, $V_{in1} = V_{in3} = 0$ (grounded), $V_{out3} =$ output voltage signal and $Q = 1$: $C_1 = C_2 = 10$ pF and $R_1 = R_2 = 1$ k$\Omega$. It is observed that 15.9 MHz with 160 mVp-p input voltage signal levels are possible without significant distortion. These simulation results are coherent with the theoretical analyses.

Conclusions

In this paper, a versatile high input impedance voltage-mode universal biquadratic filter with three-inputs and five-outputs is presented. The proposed circuit uses three plus-type DDCCs, two grounded capacitors and two resistors and offers following advantages: (i) provides five standard filter functions, that is, highpass, bandpass, lowpass, notch, and allpass filters, simultaneously, from the same configuration, (ii) needs not component matching condition to realize all filter types, (iii) high input impedance, (iv) uses only plus-type DDCCs and (v) low active and passive sensitivities. Comparisons of some reported one-input and five-outputs universal biquads are given in Table 2. Table 2 shows the features of the proposed circuits in the number of passive components used and needs not component matching conditions.

References