Design of solar insolation power logging system with ADC error testing and correction

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This study presents a low cost solar insolation meter with accurate measurement of inherent non-linear transfer characteristics of ADC. Measured values were found close to accuracy of highly sophisticated instruments (pyranometer and pyrheliometer), which are costlier for large-scale use, low commercial availability and need for a specialized knowledge for handling. Test results over a long duration under varying seasonal conditions were almost identical to those of a calibrated standard pyranometer.

Keywords: ADC error correction, Renewable energy, Solar energy, Solar radiation

Introduction
After installation of a solar power system, periodical logging of solar radiation data is mandatory to ensure sustained operation of solar system under various positions, inclination of earth and unpredictable weather conditions. Success of any solar system depends highly on accuracy of site specific solar radiation data available to the system. Manual method for ADC error measurement is very tedious and time consuming process. This study proposes a novel design for a simple, low cost solar insolation meter and logger, where a Time Tick based approach is used to measure errors in the data converter efficiently.

Experimental Section

Solar Radiation Measurement
Solar insolation is measured as

\[ GSI = DSI + DiSI \]  

where, global solar irradiance (GSI) is total solar energy obtained, direct solar irradiance (DSI) is measure of solar energy directly from the sun and diffused solar irradiance (DiSI) measures energy from sources other than sun. Eq. (1) can be expressed as

\[ GSI = DSI \cos(I) + DiSI \]  

where, \( I \) = Incident angle of beam.

Solar irradiance is measured by a transducer (PV cell or solar cell), which converts short circuit current to an equivalent voltage, which has a linear relationship with incident solar energy. While measuring this value sometimes instrumental (ADC) error might be added to measured value, leading to incorrect measurement. For an 8-bit ADC, one has a total of \( 2^8 - 1 = 255 \) levels. It is assumed that 200\(^{th}\) level has an irradiance of 1000 W/m\(^2\), whereas 255\(^{th}\) level represents full scale voltage (5V). Maximum measured solar irradiance (MMSR) is measured as

\[ MMSR = \frac{(2^N - 1) \times G}{L_G} \]  

where, \( N \), number of bits in ADC; \( G \), assumed maximum solar irradiance; \( L_G \), level at which \( G \) value is assumed. This calculation is for ideal measurement when there is no error in ADC. If there is any error, Eq. (3) becomes as

\[ MMSR = \frac{(2^N - 1) \times G}{L_G} + \text{error} \]  

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Irradiance value for 255 levels is given as:

\[ MMSR = \frac{255 \times 1000}{200} = 1250 \text{ W/m}^2 \]

**Experimental Setup**

**Instrument Components**

SIPS (Solar Insolation Power Logging System) consists of power supply circuit, input circuit, PIC, output circuit, crystal oscillator and real time clock units (Fig. 1).

**Power Supply Circuit**

Components present in power supply unit are: i) Rechargeable battery (2200 mAh current and 11.1 V); ii) B. IC7805, a voltage regulator IC to give constant 5V DC to SIPS; and iii) Noise filtering capacitors (1 µF & 10 µF) used parallel to supply to arrest noise in power supply.

**Input Circuit**

Input circuit consists of following components: i) Solar panel (SP), which receive voltage and gives to voltage divider to forward to ADC, present in PIC microcontroller; ii) Conditioned ramp source (CRS), another input to ADC, can be selected by using S/~R switch. It is used to switch input between either solar panel or CRS. These two input sources together (Fig. 2) are known as signal source module (SSM); and iii) C.3*5 matrix keyboard, in which 15 switches are placed as 3 rows and 5 columns, and used to bring SIPS to different modes. Different modes present in SIPS are: 1) Time configuration mode (TCM), used to set RTC time, date and year option; 2) Data logging mode (DLM), to log data in two types of logging (continuous DLM, in this mode solar data is logged continuously; and single time DLM, in this mode data is logged only once); and 3) Ideal time ticks calculation mode (ITTCM), which by using signal source module for ramp signal calculates ideal time ticks, and used for ADC error correction.

**PIC**

PIC 16F877A (programmable interface controller) is a 40 pin RISC CPU, which is used to record analog data, give control information & data to LCD display, and monitor RTC (real time clock). It has inbuilt ADC with 5 ports to get input and send output. These ports connection with other external components are given as follows: Port A - It has five pins (RA0 - 1st pin is used to get input from either SP or CRS; RA4 - 5th pin used to get counter input); Port B - It is connected to a 3*5 matrix keyboard, where 3 pins are used as input and 5 pins as output; Port C - In this port, first three pins (RC0, RC1, RC2) are used as LCD RS (Register Select) pin, LCD R/W (Read/Write) pin and LCD En (Enable) pin, respectively, RC3 pin is used as a clock generator for both RTC and EEPROM SCL (Serial Clock), and RC4 pin is used as a serial data for both RTC and EEPROM SDA (Serial Data for); Port D - All pins present in this port are directly connected to data bus of LCD display unit; and Port E - This port has 3 pins (RE0, RE1 pins are connected to two switches S1 and S2, and RE2 is connected to S/~R switch).

**Output Circuits**

Output circuits have a LCD display and a 24C512 external interfaced memory. In this, SIPS system 16*2 LCD displays sampled analog data, different modes in
SIPS, RTC time and number of sampled and stored data in EEPROM 24C512. By using FC concept, data is stored. Main advantage of using this concept is usage of lesser number of pins to transfer data.

Crystal Oscillator and Real Time Clock Units
RTC DS1307 IC is used to show real time in seconds, minutes, hours, date of month, month, day of week, and year with leap-year compensation and valid up to 2100. Crystal oscillator (20 MHz) is heart of PIC controller. Serial port is used to program microcontroller from PC at the first time. Max232 IC is used as an interface between PC and microcontroller.

ADC Error Correction
To reduce error introduced by ADC, system is calibrated by applying either sine wave source or linear ramp source to ADC. In present SIPS system, a digitally switchable ramp source (DSRS) is used as input (Fig. 3). DSRS generates an adaptive slope of ramp signals. To generate linear ramp, there are different methods (Mixed-Signal, SSLAR Ramp signal, Low cost adaptive ramp generator and high precision ramp generator), whose slope depend upon their passive devices. But present system requires a ramp signal with dynamically variable slope to find error of ADC. Initially, switch S1 is in off state. Slope detector output is connected to microcontroller pin. Microcontroller polls the value of \( V_{lt,o} \). Cntr variable begins counting if and only if \( V_{lt,o} = 0 \) and \( Cntr =0 \). Cntr variable counts ideal time ticks for total ramp signal. This data is stored in a memory and ideal time tick values are computed and stored.

Slope detector circuit (Fig. 4) is used to detect ramp signal level by using two comparators. Analog ramp signal is fed as input to non inverting terminal of both comparators, whereas corresponding threshold values are passed to inverting terminals. Voltages are determined by required voltage level of ramp source. This circuit gives output as high only when lower comparator output is high and upper comparator output is low. This output is given to counter present in controller for finding ideal time ticks, after which capacitor is discharged to 0V by using another switch S2 that is connected across capacitor (Fig. 3).

After setting required slope ramp signal as input, \( S/R \) switch is brought down to low state (\( S/R=0 \)). Now, SIPS system will operate in Practical Time Ticks (tt) Calculation mode. Desired slope ramp input is applied to ADC. SIPS will calculate Practical Time Ticks (Fig. 5) of each code occurrence (\( 1\text{Code} =1\text{LSB Size} \)) and store it in memory. First ramp will start from \( V_{\text{min}} \) (0V) and linearly increasing up to \( V_{\text{max}} \) (5V). Initially, counter is loaded with zero. This counter value will increase if one gets a same sample output. Else this value is stored in a memory location corresponding to input code. Counter is again initialized to zero and above process is continued until occurrence of maximum code or \( V_{\max} \) (For an 8bit ADC, maximum code = \( 2^8-1 = 255 \)). Samples taken from readings may be simplified as a second order equation as

\[
\begin{align*}
\sum_{i=1}^{n} x_i y_i & = a_0 \\
\sum_{i=1}^{n} x_i & = a_1 \\
\sum_{i=1}^{n} x_i^2 & = a_2 \\
\sum_{i=1}^{n} x_i^3 & = a_3 \\
\sum_{i=1}^{n} x_i^4 & = a_4
\end{align*}
\]

where, \( n \) is number of collected samples, \( y_i \) is correlation factor. \( x_i \) is measured input \( V_{IN} \).
From Eq. (5), error of an ADC is modeled. From this observation, values are found of coefficients \((a_0, a_1, a_2)\) required to model error. After error model is computed, any input is correspondingly corrected using Eq. (5). The data to be corrected is input \(x\) in Eq. (5).

**Results and Discussion**

SIPS system output with and without correction (Fig. 6a) compares well with ideal pyrheliometer output using present ADC error corrected output (Fig. 6b). Thus from obtained output, as time increases, received solar radiation increases, at noon obtained solar radiation is maximum, and a minimum is obtained at 6.00 pm. Further from output, nonlinear behavior of ADC affects obtained solar radiation data. In error plot (Fig. 7), SIPS system measurements compared with pyrheliometer for every 10 min interval and it is plotted. From error correction algorithm, corrected output is almost equal to output obtained by pyrheliometer.

SIPS system can be used for long term data logging and correlating the results for future application using fuzzy logic\(^\text{12}\). Further, these insolation measurements are highly helpful in systems where solar data needs to be constantly monitored and verified\(^\text{13}\). For designed system uses an ADC for data conversion, a microcontroller for data acquiring, analyzing and correction, an EEPROM

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**Fig. 5 — Practical time tick calculation**

**Fig. 6 — a) Practical values vs error corrected values; b) Error corrected values vs pyrheliometer values**

**Fig. 7 — Error plot**
for data logging and a display/keypad for displaying measured data and for fixing settings. SIPS system also concentrates on ADC error testing and its correction to bring measured reading closer to calibrated standard instruments like pyrheliometer.

Conclusions

A low cost solar insolation system with ADC error correction is presented. Error corrected output of ADC is found almost equal to practical high cost pyrheliometer output. Proposed SIPS system is a low cost system, where cost of entire system sans solar sensor module is range of few thousand rupees, while cost of existing systems ranges from few ten thousands to lakhs rupees. Automatic data logging is another beneficial feature of this system. Further, SIPS system is easily portable. It can be interfaced to PC via serial port, to get data logged in memory. SIPS system also gives starting time and interval between two data logging. This feature is highly useful for scientific research and climatic change monitoring system. Life time expectancy of SIPS system is based on EEPROM read/write cycles and data retention period.

References